1. Multiple-choice questions:

(1) If both inputs of a 2-input XOR gate are 1s, what is the output of this XOR gate?
(a) 0 (b) 1 (c) Unknown (d) Don't Care

(2) The (unsigned) binary equivalent of 20.625 is:

(a) 01010.111 (b) 001010.111 (c) 010100.101 (d) 001010.101

(3) Circle the 4-bit signed 2's complement representation of -3.

(a) 1011 (b) 0011 (c) 1101 (d) 1100

(4) The simplest Boolean expression for $(\overline{a}+\overline{b})(\overline{a}+b)$ is:

(a) $a \oplus b$ (b) $\overline{a}$ (c) $\overline{a}+b$ (d) b

(5) Select the simplest Boolean expression for

$$f = \overline{A}\cdot\overline{B}\cdot\overline{C} + \overline{B}\cdot C + A\cdot\overline{B}\cdot\overline{C} + A\cdot B\cdot C + A\cdot\overline{C}$$

(a) $A+\overline{A}\overline{B}$ (b) $A+\overline{B}$ (c) C+B (d) $A\cdot\overline{C}$

2. Given

$$f(A,B,C) = \sum m_i(1,5,6,7)$$

(a) Express f in a canonical sum of products form.
(b) Use Boolean logic to minimize f in a sum of products form.
(c) Implement f using a 8:1 Multiplexer.

3. Given

$$f(A,B,C) = \prod M_i(0,1,2,4,5,6)$$

(a) Express f in a canonical product of sums form.
(b) Use Boolean logic to minimize f in a product of sums form.
(c) Implement f using a 4:1 Multiplexer.

4. Map the following functions and find the minimal S. O. P. or P. O. S. forms.

(a) $\overline{A}\cdot C + A\cdot\overline{B}\cdot C + A\cdot B + \overline{A}\cdot B\cdot\overline{C}$

(b) $(A+B)\ (\overline{A}+\overline{B})\ (A+\overline{B}+\overline{C})$

5. Use the K-map method to find the minimized product of sums expressions for the following Boolean functions:

(a) $f(A,B,C) = (A \odot B)\cdot C$

(b) $f(A,B,C,D) = \sum m_i(1,2,4,5,10,14) + \sum d_i(0,6,13,15)$

where $\sum d_i(...)$ means the sum of minterms that correspond to *don't care* outputs.

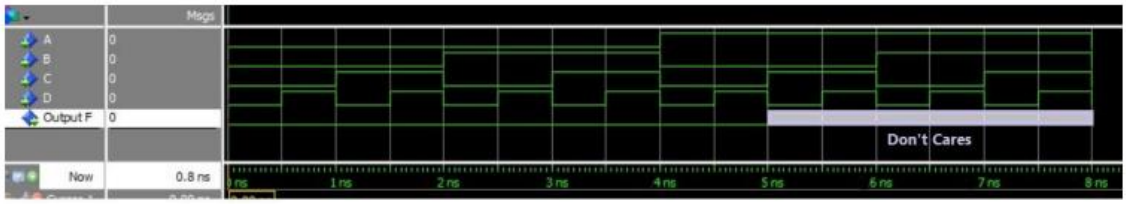
6. Draw schematics for the following expressions mapped into
   (a) NAND-only networks,
   (b) NOR-only networks.
   Assume that literals and their complements are available.
   i) $(A \cdot B + C) \cdot E + D \cdot G$
   ii) $A \cdot \overline{B} \cdot (\overline{B} + C) \cdot \overline{D} + \overline{A}$

7. Design Question:

Design a "Banner Number Detector" that can detect the binary coded decimals (BCD) in your banner number. The circuit has 4 inputs: **A, B, C,** and **D** connected to four switches, with A being the MSB of the inputs, and D being the LSB of the inputs.

The circuit has one output **F** connected to a LED. **F** should be '**1**' when the inputs represent one of the decimals in your banner number. For example, if your Banner number is B00120088, the output F should be '**1**' when the inputs are "0000"(i.e. 0d), "0001"(1d), "0010"(2d), and "1000"(8d).

F should be '**0**' when the inputs represent other decimals, and for the combinations of the inputs that are not used for BCD, the outputs are **Don't Cares**.



Please write down your Banner number here (i.e. 8-digit number after B): B_____

(a) If the above waveform is used to represent your detector, list the time periods that the output F should be high ('1') for your Banner numbers.

Answer: e.g. 0-0.5ns, _____

(b) Use K-map to represent the function F. Making use of the Don't Cares, simply output F to the **simplest** SOP or POS format:

F= _____

(c) Is the F you obtained hazard-free or not? If not, please make it hazard-free: _____

(d) Synthesize the hazard-free function F using logic gates, then convert it to a NAND-only network. List the number of NAND gates you used here _____.