1. Design a counter that goes through the BCD sequence of **your Banner number**. You don't need to include repeated BCD(s). **For example, B00458387** has two repeated numbers '0' and '8'.
The required counting sequence is: 0000 (0d) -> 0100 (4d) -> 0101 (5d) ->1000 (8d) -> 0011(3d) -> 0111 (7d), then back to 0000 (0d). The underlined numbers are skipped in the counting sequence.

(a) Using the standard design process for **synchronous** counters, show how to implement this counter using D flip-flops. Please include: state transition table, K-maps, next_state equations, and a drawing of the final circuit. Assuming literal complements are available. [6 pts]

(b) Is your counter designed in part (a) self-starting or not? Draw the state transition diagram including every possible state. [3 pts]

(c) Implement one DFF used in part (a) with Master-Slave RS latches. [3 pts]

(d) Implement one RS latch used in part (c) with logic gates. Please include asynchronous "Preset" and "Clear" for the RS latch. Assume multiple-input logic gates allowed. [3 pts]

2. Partially design a pattern detector that can detect the **largest and the smallest non-zero** BCDs **in your Banner number**; **overlapping allowed**. **For example**: B00458387: the smallest non-zero BCD is "0011" for 3d, and the largest is "1000" for 8d. The pattern detector has one serial-input **X** and one output **Z**. The output Z=1 for one clock cycle when either "0011" or "1000" has been detected. At all other times Z is set to 0.

(a) Derive a symbolic state diagram for your pattern detector; reduce redundant states. [4 pts]

(b) Assign binary representations for all states. [3 pts]

(c) Identify at least one alternative approach for the design of this pattern detector. Justify your choice of FSM and the binary state assignment. [3 pts]

No need to implement this pattern detector further than the binary assignment step.