1. (a) Using the minimum 2-level SoP logic required, design a sequential circuit with three T flip-flops, A, B and C, and two inputs E and X that performs as follows:
   - If E = 0 the circuit remains in the same state regardless the value of X,
   - When E = 1 and X = 1 the circuit goes through the state transitions 000 to 001 to 010 to 011 to 100 back to 000, and repeats,
   - When E = 1 and X = 0 the circuit goes through the state transitions 111 to 110 to 101 to 100 to 011 back to 111, and repeats.

   (b) Is the countup self-starting, *i.e.* if X remains at 1? Justify. Include state transition diagram.

   (c) Is the countdown self-starting, *i.e.* if X remains at 0? Justify. Include state transition diagram.

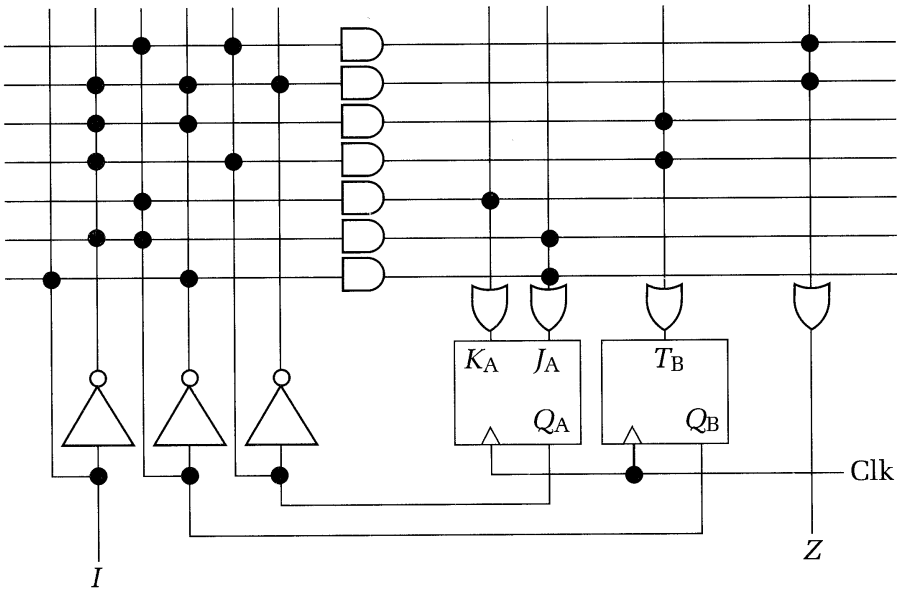
2. The finite state machine (FSM) shown in the figure below is implemented with one toggle (T) flip-flop and one JK flip-flop. It has one input I and one output Z. The combinational logic required for the next state and output functions is implemented by a PLA structure.

   (a) Write the logic expressions for J_A, K_A, T_B and Z.

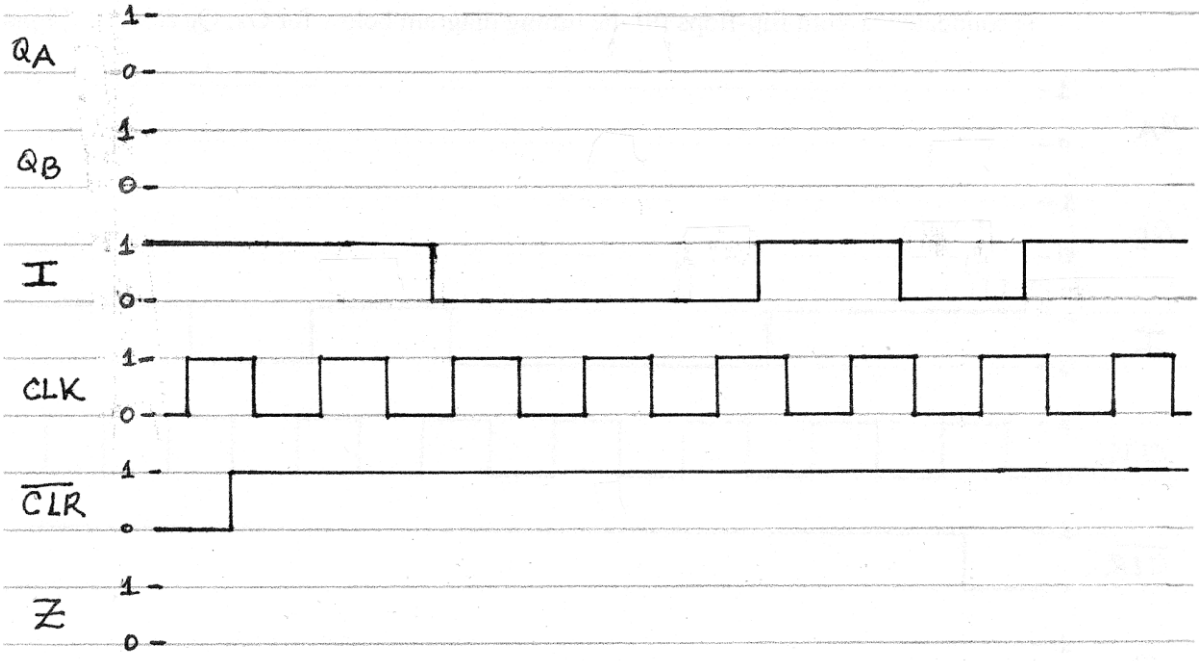
   (b) Which of the two types of FSM seen in classes is this? Justify.

   (c) Obtain the state transition table including the output Z.

   (d) Draw the complete state transition diagram of the FSM.



   (e) Assuming the $\overline{PR}$ is deasserted (HIGH) and the active-low clear $\overline{CLR}$ below is connected to both flip-flops fill the timing diagram below for Q_A, Q_B & Z.



3. Design a Mealy finite state machine with input X and output Z. The output Z should be asserted for one clock cycle whenever the sequence ….0111 or …1000 has been input on X. The patterns may overlap. For example, X = ...0000111000…should generate the output stream Y = …0000001001…

(a) Complete the state diagram for the sequence detector, without concern for state minimization;

(b) Minimize the number of states;

(c) Use the state assignment guidelines to obtain a good state assignment for the reduced state machine.

(d) Implement your encoded, reduced state table and show all the minimized logic equations for the next state and outputs.

(e) Implement this Mealy finite state machine with DFFs.