DALHOUSIE UNIVERSITY

Department of Electrical & Computer Engineering

ECED 2200 - Digital Circuits

Final Examination **Winter 2015**

Name: ______________________________________ **Student ID:** __________________

Marks: Total marks out of 45

Question	Subject	Worth	Marks
1	Gates and Boolean algebra	8	
2	Arithmetic circuit design	8	
3	Decoders and multiplexers	7	
4	Synchronous & Asynchronous counters	12	
5	Registers	10	
Total		45	

Q1. The Boolean expression given below describes the XNOR function of variables **a** and **b**.

$$f = ab + a'b'$$

(a) Synthesize the XNOR function using AND, OR and NOT gates. [2 pts]
(b) Convert the circuit from (a) to NOR-only networks (Note: **a'** and **b'** are not available). [2 pts]
(c) Using Boolean algebra to implement the function with no more than 4 NOR logics. [2 pts]
(d) Draw the new circuit implemented with 4 NOR gates. [2 pts]

Q2. A half adder circuit has two inputs **a** and **b**, and two outputs **S** and $\mathbf{C_o}$. A full adder circuit has three inputs **a**, **b**, $\mathbf{C_{in}}$ and two outputs **S** and $\mathbf{C_o}$.

(a) Design a half adder that calculate the sum of **a** and **b**. [2 pts]
(b) Design a full adder using two half adders to calculate the sum of **a**, **b**, and $\mathbf{C_{in}}$. [2 pts]
(c) Show in 8-bit binary notation the arithmetic operation of 30+(-19). [2 pts]
(d) Design a 8-bit chained adder using full adder as components. [2 pts]

Q3. **(** a) Implement the following Boolean functions using 8:1 multiplexers: [2 pts]

i) $f_1(A,B,C) = \sum m_i(0,5,6,7)$

ii) $f_2(A,B,C) = \prod M_i(0,3,6)$.

We are also told that the input combinations ABC = 100 and ABC = 111 are not of concern (don't cares) for f_2.

(b) Implement the same Boolean functions f_1 & f_2 given above using 4:1 multiplexers. [2 pts]

(c) Implement the Boolean functions below using one 3:8 decoder and three OR gates. Specify all the decoder inputs. [3 pts]

i) $f_1(A,B,C) = \sum m_i(5,6,7)$

ii) $f_2(A,B,C) = \overline{A}\cdot\left(B+\overline{C}\right)$

iii) $f_3(A,B,C) = \overline{A}\cdot C + A\cdot\overline{B}\cdot\overline{C}$

Q4. A binary decade up-counter goes through the sequence 0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, 0000, 0001, …

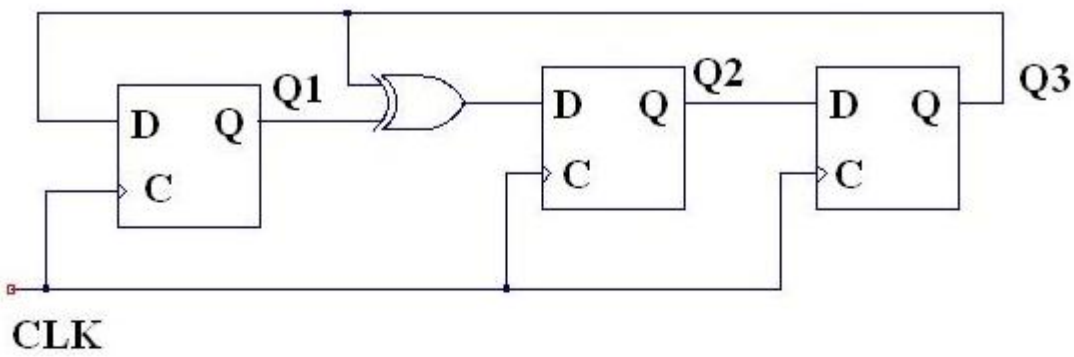
(a) Using the standard design process for synchronous counters, show how to implement this counter using T flip-flops.
Include: state transition table and a drawing of the final circuit. [3 pts]

(b) Check whether the counter is self-starting or not? Draw the state transition diagram including every possible state. [3 pts]

(c) Build an asynchronous (ripple) decade up-counter by modifying a 4-stage ripple binary up-counter using T flip-flops. [3 pts]

(d) Sketch the timing diagram of the counter built in (c) for 12 CLK periods. Assume all flip-flops were cleared during the clock cycles preceding time t=0. Include:
- The waveforms CLK_A, CLK_B, CLK_C, & CLK_D, (i.e. the CLK inputs of each flip-flop)
- The waveforms Q_A, Q_B, Q_C, & Q_D, (i.e. the outputs Q of each each flip-flop) [3 pts]

Q5. The synchronous circuit given below is a linear feedback shift register (LFSR).



(a) Complete the next state equations (i.e. $Q1^+$, $Q2^+$, $Q3^+$), one for each stage (flip-flop). [3 pts]
(b) Assuming that $Q_1Q_2Q_3 = 001$ at t = 0 (initialization). Determine the contents of the LFSR after the first, second, third, …… eighth clock cycles and fill in the table given below. [3 pts]

CLK	Q1	Q2	Q3
	0	0	1
1			
2			
3			
4			
5			
6			
7			
8			

(c) Check whether the counter is self-starting or not? Draw the state transition diagram including every possible state. [2 pts]
(d) What are the contents of Q1, Q2, and Q3 after clocks 97 and 168? [2 pts]

Excitation Table

Q	Q+	R	S	J	K	T	D
0	0	X	0	0	X	0	0
0	1	0	1	1	X	1	1
1	0	1	0	X	1	1	0
1	1	0	X	X	0	0	1

Basic Boolean Identities

	Identity	Comments
1.	$A+0=A$	Operations with 0 and 1
2.	$A+1=1$	Operations with 0 and 1
3.	$A+A=A$	Idompotent
4.	$A+\overline{A}=1$	Complementarity
5.	$A\cdot 0=0$	Operations with 0 and 1
6.	$A\cdot 1=A$	Operations with 0 and 1
7.	$A\cdot A=A$	Idompotent
8.	$A\cdot\overline{A}=0$	Complementarity
9.	$\overline{\overline{A}}=A$	Involution
10.	$A+B=B+A$	Commutative
11.	$A\cdot B=B\cdot A$	Commutative
12.	$A+(B+C)=(A+B)+C=A+B+C$	Associative
13.	$A\cdot(B\cdot C)=(A\cdot B)\cdot C=A\cdot B\cdot C$	Associative
14.	$A\cdot(B+C)=(A\cdot B)+(A\cdot C)$	Distributive
15.	$A+(B\cdot C)=(A+B)\cdot(A+C)$	Distributive
16.	$A+(A\cdot B)=A$	Absorption
17.	$A\cdot(A+B)=A$	Absorption
18.	$(A\cdot B)+(\overline{A}\cdot C)+(B\cdot C)=(A\cdot B)+(\overline{A}\cdot C)$	Consensus
19.	$\overline{A+B+C+...}=\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot...$	De Morgan
20.	$\overline{A\cdot B\cdot C\cdot...}=\overline{A}+\overline{B}+\overline{C}+...$	De Morgan
21.	$(A+\overline{B})\cdot B=A\cdot B$	Simplification
22.	$(A\cdot\overline{B})+B=A+B$	Simplification