DALHOUSIE UNIVERSITY

Department of Electrical & Computer Engineering

ECED 2200 - Digital Circuits

**Final Examination** **Winter 2016/2017**

**Name:** _____ **Student ID:** _____

## **Marks:** Total marks out of 45

| Question | Subject | Worth | Score | Outcome Achievement |
|---|---|---|---|---|
| 1 | Multiple-choice questions | 10 | | ----- |
| 2 | Counters | 12 | | ----- |
| 3 | Sequential circuit | 9 | | ----- |
| 4* | Finite State Machines | 14 | | |
| Total | | 45 | | ----- |

*Note: Question 4 is designed to evaluate course outcome 04B (i.e. Conceptualize and evaluate alternative approaches; perform appropriate design to fit requirements).

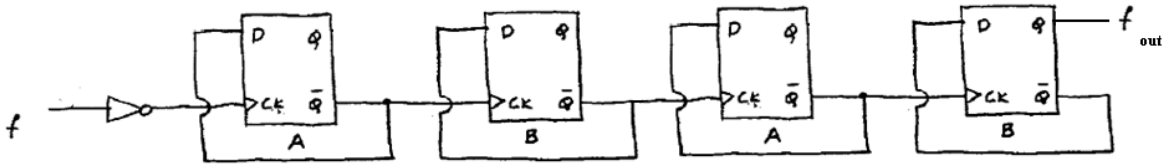
**Excitation Table**

| Q | Q+ | R | S | J | K | T | D |
|---|---|---|---|---|---|---|---|
| 0 | 0 | X | 0 | 0 | X | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | X | 1 | 1 |
| 1 | 0 | 1 | 0 | X | 1 | 1 | 0 |
| 1 | 1 | 0 | X | X | 0 | 0 | 1 |

**Q1.** Multiple-choice questions. Circle **ONLY ONE** that apply. [1 pt each]

(1) How can the cross-coupled NAND RS latch used in Lab4 be made to have active-HIGH inputs?
(a) It can't be done (b) Invert the S-R inputs (c) Invert the Q (d) Invert the clock

(2) Four (4) D flip-flops are connected in tandem as a Frequency Divider. For a 2 MHz square wave input frequency, determine the frequency of the output:




(a) 1MHz (b) 500 kHz (c) 125 kHz (d) None of the above

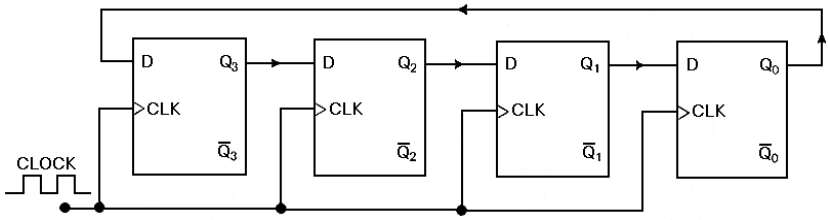
(3) To implement a T flip-flop using a JK flip-flop:
(a) J=K=1 (b) J=T, K=0 (c) J=T, K=T' (d) J=K=T

(4) A simple memory component can be implemented from:
(a) cross-coupled ANDs (b) cross-coupled NORs (c) cross-coupled XORs (d) cross-coupled ORs

(5) How many address bits (i.e. the total of row-select lines and column-select lines) would be required to address 16 x 16 RAM cells?
(a) 4 (b) 8 (c) 16 (d) 256

(6) The bit sequence 0010 is serially entered (right-most bit first) into a 4-bit parallel out shift register that is initially clear. What are the Q outputs after two clock pulses?
(a) 1000 (b) 0010 (c) 0000 (d) 0001

(7) For a 4-bit ring counter as shown below, one of the FFs is preset with a 1 and all others are cleared to 0s. How many states does this ring counter have?




(a) 4 (b) 8 (c) 15 (d) 16

(8) If we add an inverter to the feedback path of the above ring counter, we have a Johnson counter. On the fifth clock pulse, a 4-bit Johnson counter sequence is $Q_3$= 0, $Q_2$=1, $Q_1$=1, $Q_0$=1. On the sixth clock pulse, the $Q_3Q_2$ $Q_1$ $Q_0$ sequence is _____.
(a) 1011 (b) 1000 (c) 0011 (d) 0001

(9) How many flip-flops are necessary to design a state machine with 25 states?
(a) 4 (b) 5 (c) 25 (d) $2^{25}$

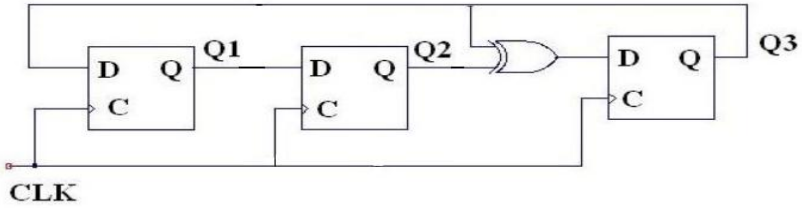
(10) Which type of finite state machines has outputs that will only change on the edge of a clock pulse?
(a) Moore (b) Mealy (c) Mealy-Moore (d) None of the above

**Q2. (a)** Design a **synchronous** up counter that goes through the sequence of 000, 001, 010, 011, 100, 101, 000, 001, …using JK FFs. Show your design steps and draw the final circuit. [4 pts]

**(b)** Is the counter designed in part (a) self-starting or not? Draw the complete state diagram. [1 pt ]

**(c)** Redesign the counter in part (a) as an **asynchronous** up counter using falling edge triggered JK FFs, **without** using the CLEAR function of the FFs (i.e. modify J, K, and clock for the desired sequence). [4 pts]

**(d)** The synchronous circuit given below is a pseudo-random counter: [3 pts]




(d1) Complete the next state equations (i.e. Q1+ , Q2 + , Q3 + ), one for each stage (flip-flop).

(d2) $Q_1Q_2Q_3$ = 001 at initialization. Is the counter self-starting? Draw the state transition diagram.

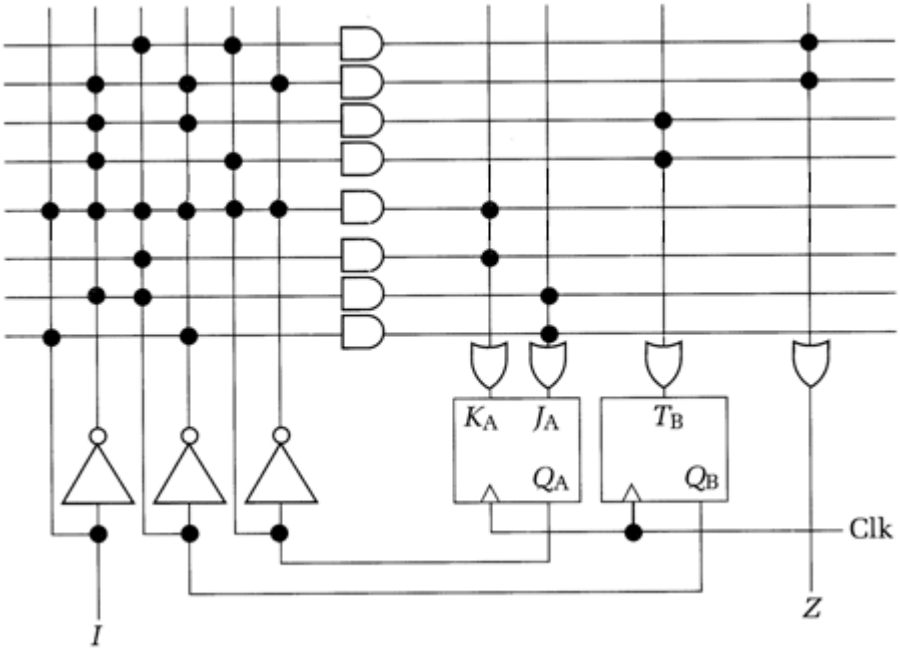
(d3) What are the contents of Q1, Q2, and Q3 after clocks 20 and 100?

**Q3.** The FSM shown below has one input I and one output Z. The combinational logic required for the next state and output functions is implemented by a PAL structure.

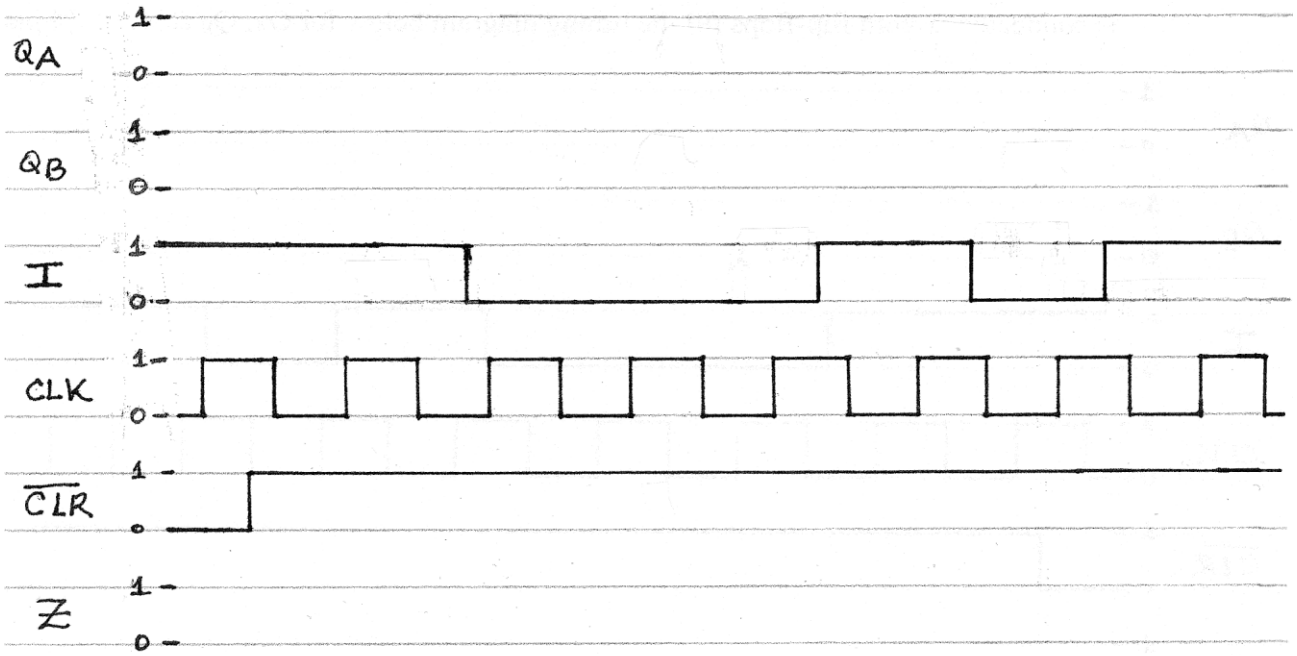
(a) Write the logic expressions for $J_A$, $K_A$, $T_B$ and Z. [2 pts]

(b) Which of the two types of FSM seen in classes is this? Justify. [1 pt]

(c) Obtain the state transition table including the output Z; draw the state transition diagram. [3 pts]




(d) Assuming an active-low clear $\overline{\text{CLR}}$ is connected to both flip-flops, fill the timing diagram below for $Q_A$, $Q_B$ & Z. [3 pts]




**Q4.** A pattern detector has one input X and one output Z. The output Z=1 whenever either of the sequences "110" or "001" has been detected, overlapping allowed. At all other times Z is set to 0. Note that the machine does not reset once one of the two sequences is detected.

(a) Implement this pattern detector as a Moore or Mealy FSM; justify your decision. [2 pts]

(b) Derive the symbolic state table and reduce redundant states. Draw the reduced state transition diagram. [4 pts]

(c) Use the state assignment guidelines learned in class to obtain a good state assignment for this FSM. [3 pts]

(d) Implement your encoded FSM using D FFs; show the minimized next-state equations and output Z. [4 pts]

(e) Draw the pattern detector circuit. [1 pt]