ECED 2200 Multiplexers and Flip-Flop Exercise

1. Implement F(A, B, C) = ∑ (1,3,5,6) with a 4:1 multiplexer

2. Implement F(A, B, C, D) = ∑ (0, 1,3,4,8,9,15) with a 8:1 multiplexer

3. If you only have a 4:1 MUX available, can you implement the function, F, defined by the truth table given below? Draw the MUX and indicate the inputs.

Q3 \ Q1Q2		00	01	11	10
	0	0	1	1	0
	1	1	0	0	1

4. A binary decade up-counter goes through the sequence 0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, 0000, 0001, …

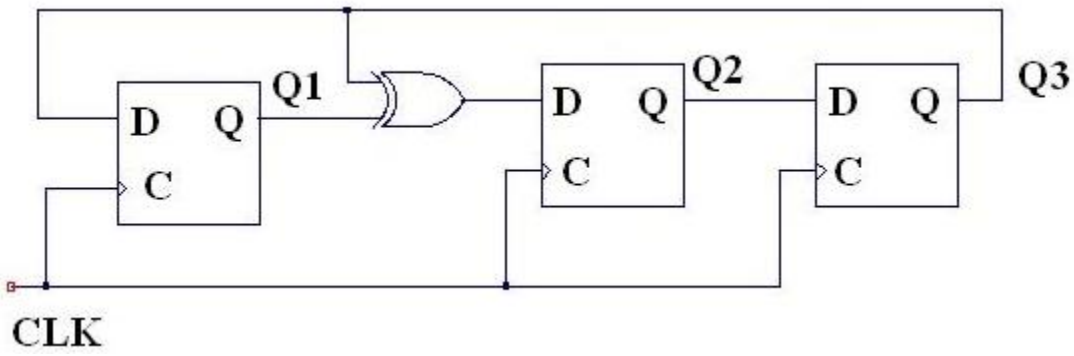
(a) Using the standard design process for synchronous counters, show how to implement this counter using T flip-flops.
Include: state transition table and a drawing of the final circuit.

(b) Check whether the counter is self-starting or not? Draw the state transition diagram including every possible state.

(c) Build an asynchronous (ripple) decade up-counter by modifying a 4-stage ripple binary up-counter using T flip-flops.

(d) Sketch the timing diagram of the counter built in (c) for 12 CLK periods. Assume all flip-flops were cleared during the clock cycles preceding time t=0. Include:
- The waveforms CLK_A, CLK_B, CLK_C, & CLK_D, (i.e. the CLK inputs of each flip-flop)
- The waveforms Q_A, Q_B, Q_C, & Q_D, (i.e. the outputs Q of each each flip-flop)

5. The synchronous circuit given below is a linear feedback shift register (LFSR).



(a) Complete the next state equations (i.e. $Q1^+$, $Q2^+$, $Q3^+$), one for each stage (flip-flop).
(b) Assuming that $Q_1Q_2Q_3 = 001$ at t = 0 (initialization). Determine the contents of the LFSR after the first, second, third, …… eighth clock cycles and fill in the table given below.

CLK	Q1	Q2	Q3
	0	0	1

1			
2			
3			
4			
5			
6			
7			
8			

(c) Check whether the counter is self-starting or not? Draw the state transition diagram including every possible state.
(d) What are the contents of Q1, Q2, and Q3 after clocks 97 and 168?

6. Implement a 4-bit bidirectional shift register with parallel load using DFFs and 4:1 MUXs.