VARIES by

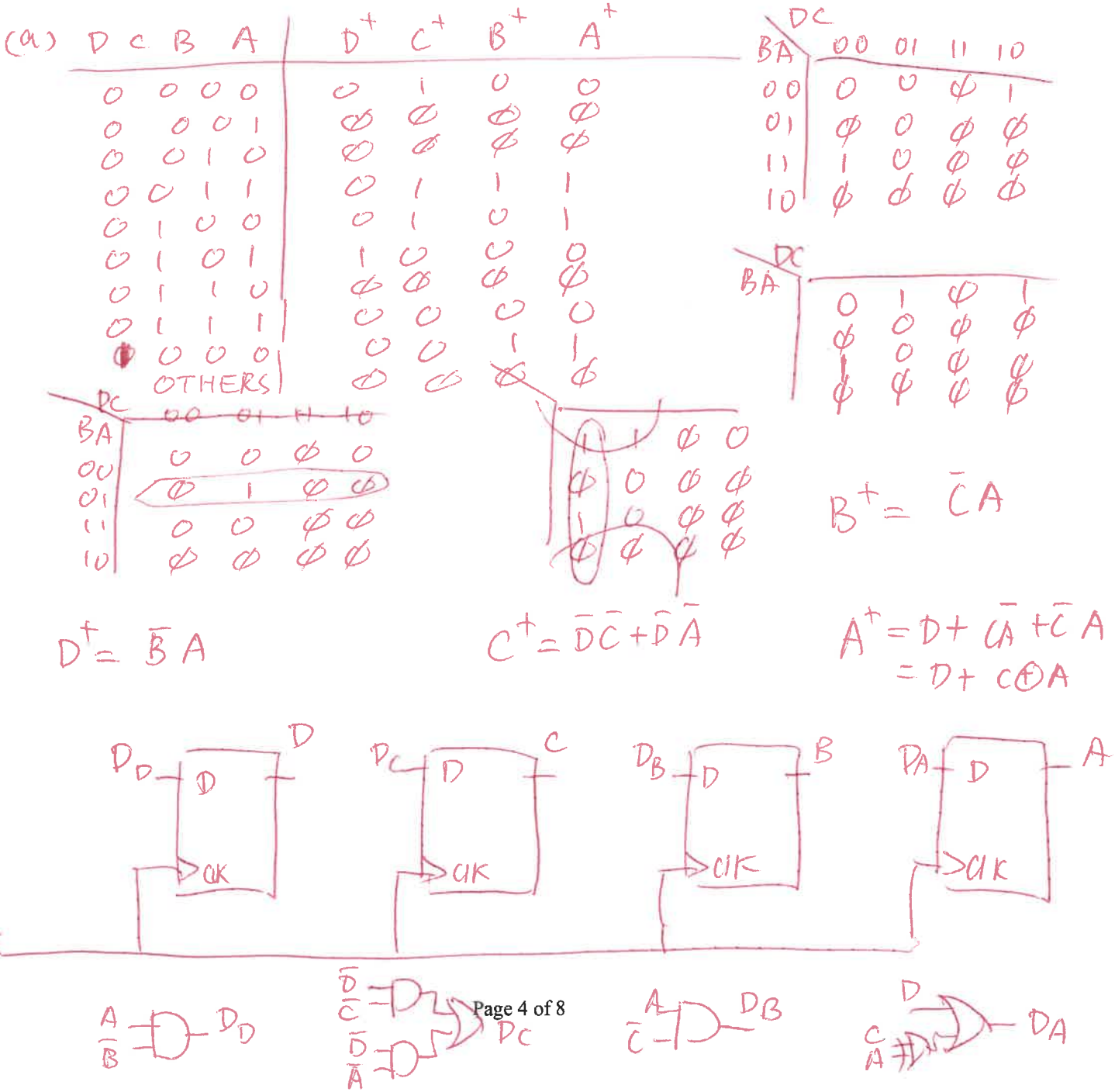
Q2. Design a counter that goes through the BCD sequence of **your Banner number**. You don't need to include repeated BCD(s). **For example, B00458387** has two repeated numbers '0' and '8'. The required counting sequence is: 0000 (0d) -> 0100 (4d) -> 0101 (5d) ->1000 (8d) -> 0011(3d) -> 0111 (7d), then back to 0000 (0d). The underlined numbers are skipped in the counting sequence.

(a) Using the standard design process for **synchronous** counters, show how to implement this counter using D flip-flops. Please include: state transition table, K-maps, next_state equations, and a drawing of the final circuit. Assuming literal complements are available. [6 pts]

(b) Is your counter designed in part (a) self-starting or not? Draw the state transition diagram including every possible state. [3 pts]

(c) Implement one DFF used in part (a) with Master-Slave RS latches. [3 pts]

(d) Implement one RS latch used in part (c) with logic gates. Please include asynchronous "Preset" and "Clear" for the RS latch. Assume multiple-input logic gates allowed. [3 pts]



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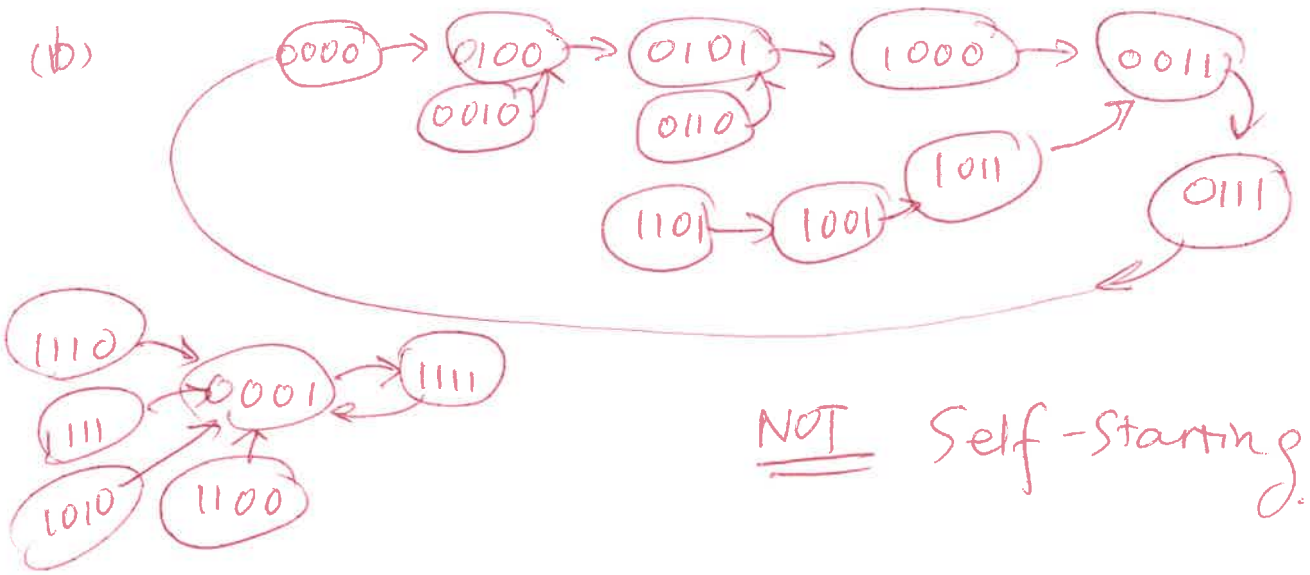
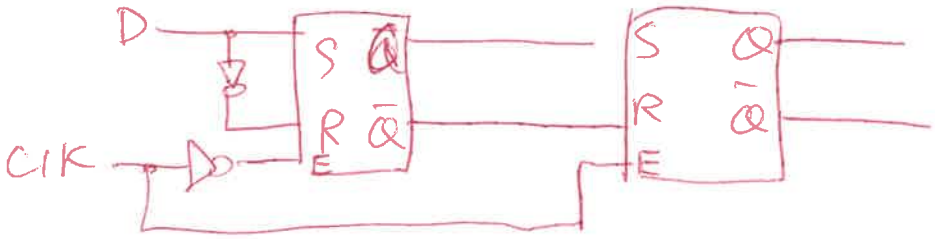
(b)



NOT Self-Starting.

(c)



(d)