Department of Electrical and Computer Engineering
Dalhousie University

ECED 2200 -- Digital Circuits

Course Outline

Course Contents	Textbook Chapters

Course Contents   **Textbook Chapters**

1. **Introduction**   **Chapter 1 and**
a) Gates   **Appendices A & B**
b) Diodes and transistors
c) Number systems
d) BCD

2. **Two-level combinational logic**   **Chapters 2 & 5**
a) Boolean algebra
b) Half adder
c) Full adder
d) Canonical forms
e) Positive and negative logic
f) Karnaugh maps

3. **Multilevel combinational logic**   **Chapter 3**
a) Conversion to NAND and NOR gates
b) Time response
c) Gate delay
d) Hazards and glitches

4. **Programmable and steering logic**   **Chapter 4**
a) Programmable array logic (PAL)
b) Programmable logic array (PLA)
c) Multiplexer / selector
d) Decoder / demulltiplexer
e) Tri-state gates

5. **Sequential logic design**   **Chapter 6**
a) Logic gate memory units
b) Timing waveforms
c) RS latch
d) D, JK, and T flip-flops
e) Conversion of one flip-flop to another
f) Debouncing switches
g) The 555 timer

6. **Sequential logic applications**   **Chapter 7**
a) Shift registers
b) Counters - divide by n, ripple, decade, ring
c) Counter design
d) Self-starting counters
e) Implementation with different types of flip-flops
f) Memory - RAM, ROM

7. **Finite state machine design**   **Chapter 8**
a) Design procedure
b) Simple example
c) Moore and Mealy machines

Mark Distribution

Labs: 20 %
Assignments: 10 %
Midterm exam: 25 %
Final exam: 45 %
Total: 100 %

Accomodation Policy for Students

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A note taker may be required to assist a classmate. There is an honourarium of $75/course/term. If you are interested, please contact OSAA at 494-2836 for more information.