DALHOUSIE UNIVERSITY
Department of Electrical & Computer Engineering
Digital Circuits - ECED 2200

Experiment 5 - Registers and Counters

Objectives:

1. To design a Serial in – Parallel out register

2. To design a Ripple counter [2 bit] (count up/count down)

3. To design a Synchronous counter [2 bit]

Theory:

Registers:

A register is a device capable of storing and shifting binary data and is typically used as a temporary storage device. Registers consist of several stages with each stage being able to hold one bit. These stages consist of a flip-flop or some other type of storage device. Shift registers are generally characterized by the method bits are inputted and outputted. Serial input / serial output registers load the bits onto the register one at a time and output bits one at a time. Serial input / parallel output registers inputs bits one at a time but an output line is placed at the exit of each stage. So with a 4-stage register four outputs would be seen. For a parallel in / serial out register bits are inputted to each stage simultaneously but the output is just one bit at a time. In a parallel input / parallel output register bits are loaded into each stage simultaneously and the output of each stage is sent to individual output lines.

Counters:

A counter is a device capable of counting electronic events such as clock pulses by progressing through a sequence of binary states. Counters usually consist of flip-flops and basic logic gates and can be asynchronous or synchronous. If the counter counts at unfixed times it is said to be asynchronous. These are commonly referred to as ripple counters. A synchronous counter is a counter that increments at a fixed time.

Part 1. Serial in – Parallel out register

Procedure:

Select an appropriate D flip-flop from Quartus II library, and implement a 4-bit serial in – parallel out register as shown on page 3. For this circuit:

1. While keeping the input constant, see what happens to the outputs with each clock transition

Part 2. Ripple Counter

Procedure:

Select an appropriate JK flip-flop from Quartus II library and implement the 2-bit ripple counter circuit as shown on page 4. In this circuit L0 and L1 are counter outputs. For this circuit:

1. Setup the circuit to count up by setting switch 3 and switch 4 appropriately (see circuit diagram).

2. What happens to the output with each clock transition?

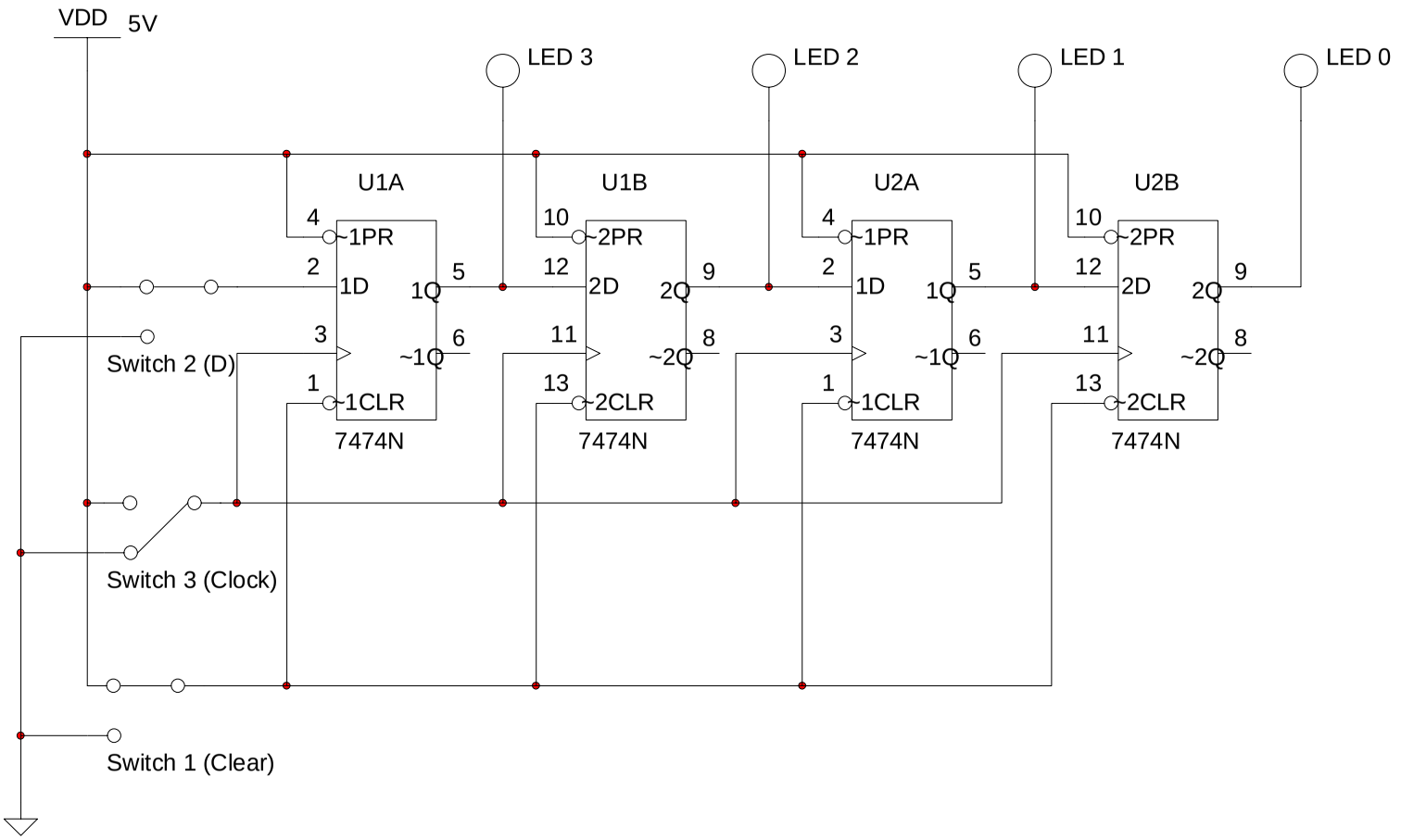
3. Setup the circuit to count down and repeat steps 1 and 2.

Part 3. Synchronous Counter

Procedure:

Implement the circuit shown on page 5. In this circuit L0 and L1 are the counter outputs. Describe what happens to the output with each clock transition.

Serial IN - Parallel OUT Register



Vcc is at Pin 14 on each IC
Ground is at Pin 7 on each IC

Title: **Lab_5_Circuit_1**		
Sheet 1 of 3		
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Checked by: **Melvin, S.**	Date **Nov 15, 2004**	Size **A**
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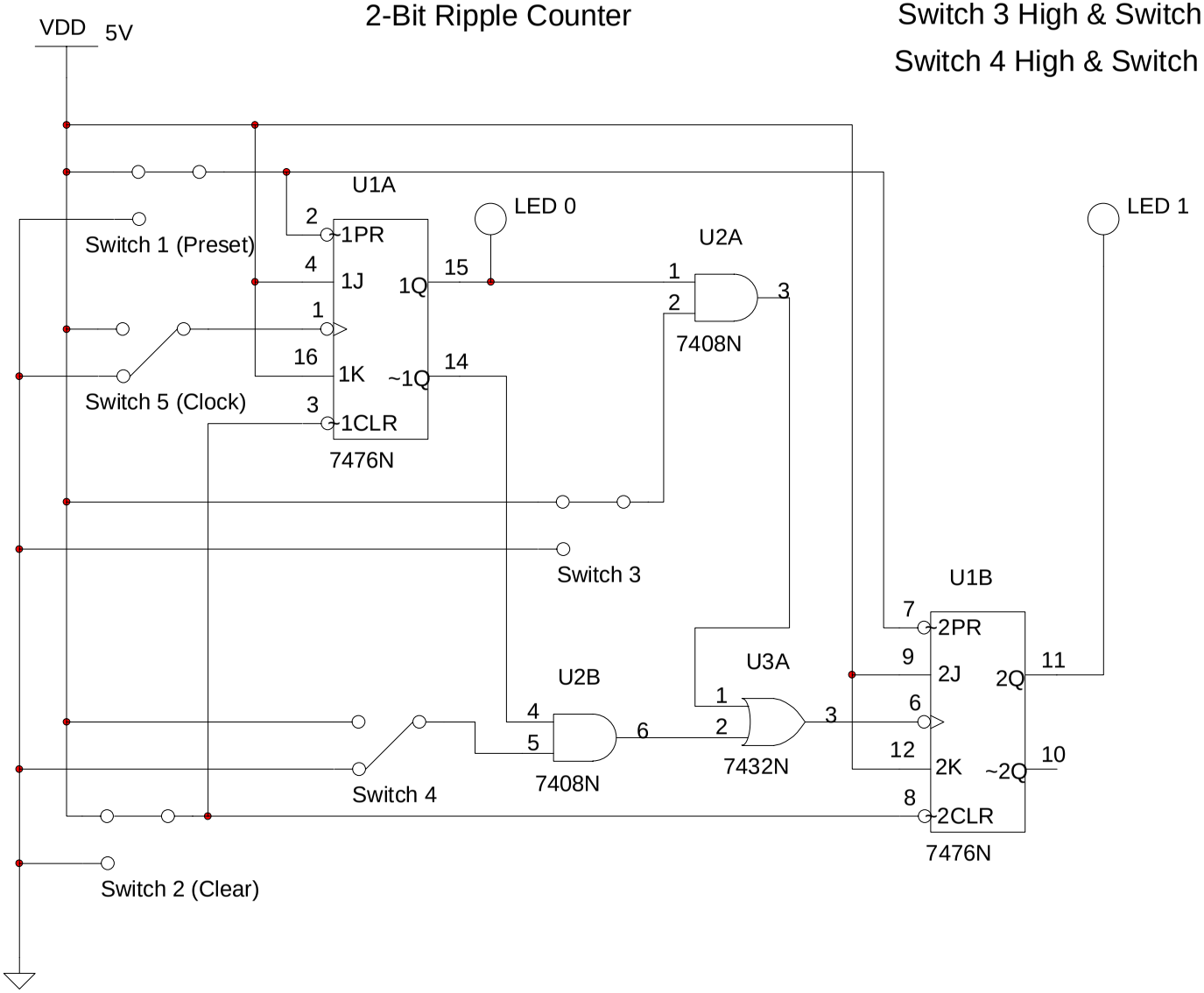
2-Bit Ripple Counter

Switch 3 High & Switch 4 Low: Count-Up

Switch 4 High & Switch 3 Low: Count-Down



Vcc is at Pin 5 on IC 7476
Ground is at Pin 13 on IC 7476

Vcc is at Pin 14 on IC 7408 & IC 7432
Ground is at Pin 7 on IC 7408 & IC 7432

Title: **Lab_5_Circuit_2**		
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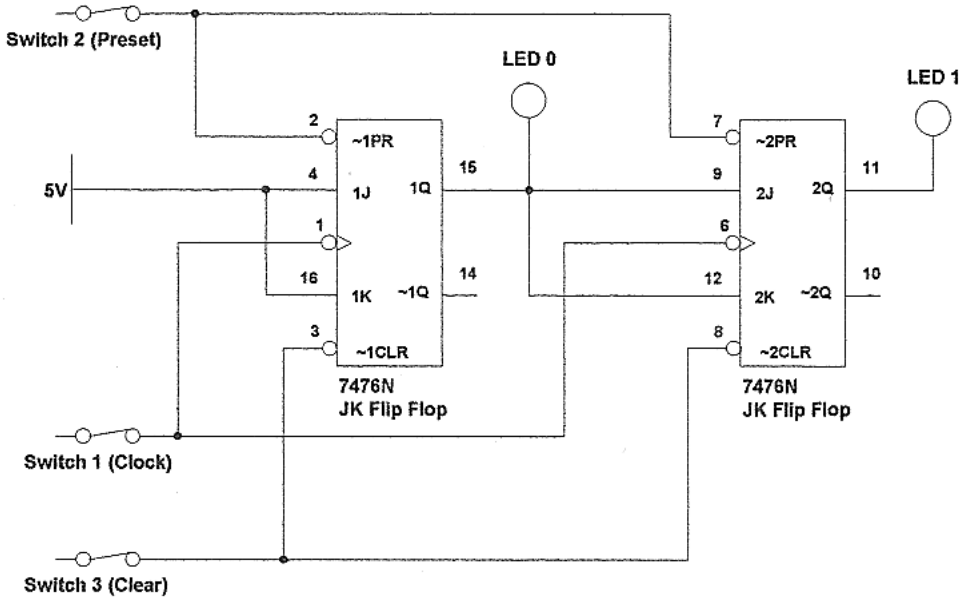
Synchronous Counter



Vcc is at Pin 5 on IC 7476
Ground is at Pin13 on IC 7476

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