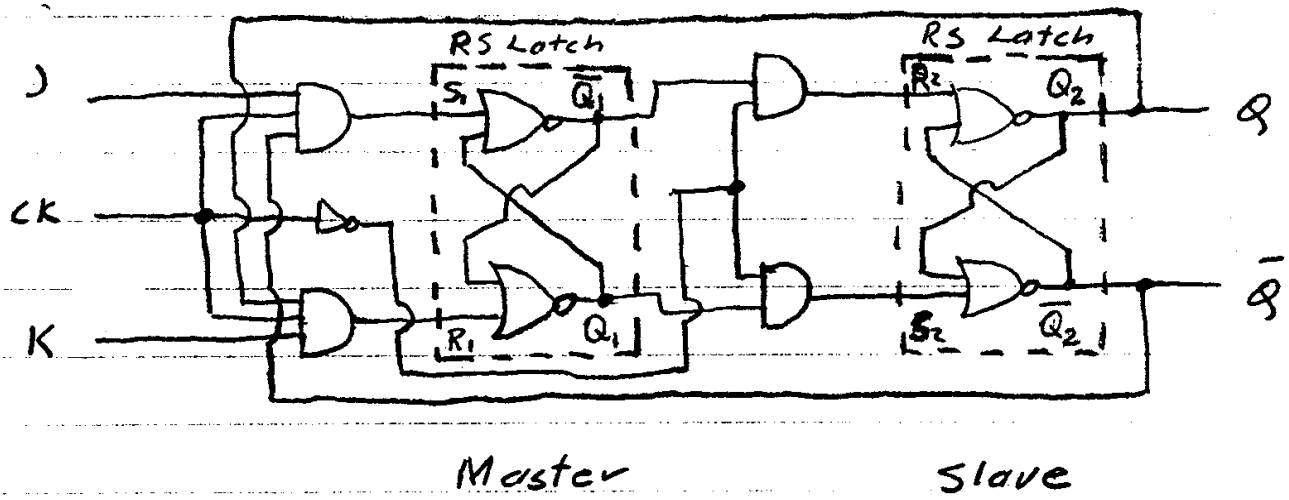
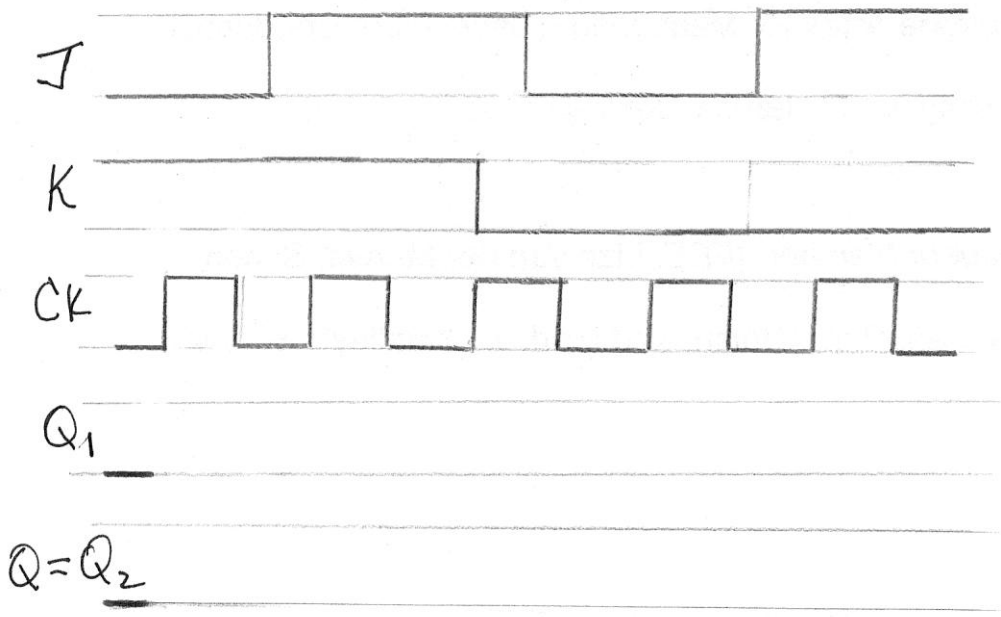
1. (a) Draw the state transition diagram of the master-slave JK flip-flop below.
   States are defined by outputs $Q\overline{Q}$. Transitions are determined by the values on input terminals JK. When do these transitions happen, on the rising or falling edge of Ck?



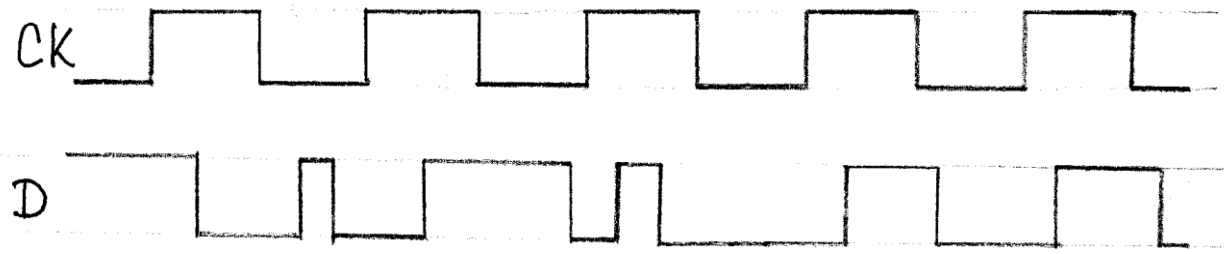
   (b) Modify the circuit to allow asynchronous PRESET and CLEAR operations.
   Are these inputs active high or active low?

2. Complete the following timing diagram for the JK flip-flop described above in 1(a) (*i.e.*, sketch Q_1 and Q). Both Q_1 and Q start at logic '0' as can be observed in the diagram.



3. (a) Draw the block diagram (two RS latches in tandem) and symbol for a D flip-flop that is "falling-edge triggered"; that is, the value of *D* is transferred to the output *Q* when *Ck* goes LOW.

   (b) Reproduce the waveforms for *Ck* and *D* (shown below) and draw the resulting waveforms for Q_1 and $Q_2 = Q$. Assume *Q* starts at logic '1'.



4. A 3-bit synchronous counter must advance through the sequence 111, 110, 101, 100, 000, 001,010, 011, 111 and then repeat. Design the counter using

   (a) JK flip-flops, and

   (c) T flip-flops.

   Are the counter implementations self-starting? Explain.

5. The following circuit contains two JK flip-flops.

   (a) Write the logic expressions for JA, KA, JB and KB.

   (b) Obtain the state transition table for the circuit.

   (c) Sketch the state transition diagram for the circuit.