

**DALHOUSIE UNIVERSITY**  
Department of Electrical & Computer Engineering  
Digital Circuits - ECED 2200

Tutorial 1. Xilinx Integrated Software Environment (ISE) Tools

**Objectives:**

1. Familiarize yourself with Xilinx ISE tools;
2. Learn about the use of 'schematic-entry' design;
3. Run a simple simulation with pre-defined stimulus;
4. Implement and generate a 7-segment BCD driver programming file;
5. Program and test your chip.

**Required Materials**

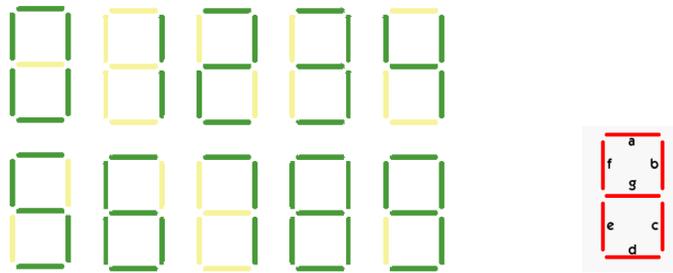
- Binary Explorer Board;
- Computer with Xilinx ISE 13.2 Webpack installed;
  - All computers in the lab have this installed.
  - This is free software so you can install on your own computer if you wish, you can download it from <http://www.xilinx.com/support/download/index.htm> - select '13.2' on the side. The file is very large so you may wish to download at school, and you are required to register to license it.
- Example project file DigitalTrainer\_Simple.zip.
  - These files contain an environment which is already setup for your lab.

**Background**

The Binary Explorer Board is a 'digital trainer' board designed by Colin O'Flynn. It contains switches and LEDs, which you can use to input 1's and 0's to a circuit, and see the response. Rather than requiring you to build circuits from discrete gates, it also contains a complex programmable logic device (CPLD) which you can design and physically implement a digital circuit with Xilinx Integrated Software Environment (ISE) tool.

**BCD to Seven-Segment decoder**

A seven-segment indicator is commonly used for representing decimal numbers. Each segment of a seven-segment display is a small light-emitting diode (LED), and - as is shown below - a decimal number is indicated by lighting a particular combination of the LED's elements:



Binary-coded-decimal (BCD) is a common way of encoding decimal numbers with 4 binary bits as shown below:

Decimal digit	0	1	2	3	4	5	6	7	8	9
BCD code - D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001

In the second part of this lab, you will program and test a circuit to drive the 7-segment display using a 4-bit BCD signal.

### Procedure

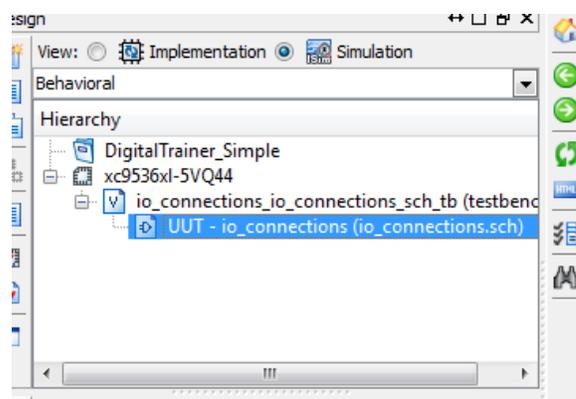
The Xilinx tools can be setup to support hundreds of different devices and several ways of entering your design. For this tutorial, a reference file ‘DigitalTrainer\_Simple.zip’ containing a project file that maps to the existing hardware has been extracted into the course folder. Open the [DigitalTrainer\\_Simple](#) folder.

#### Part 1. Simulation with ‘schematic-entry’ design

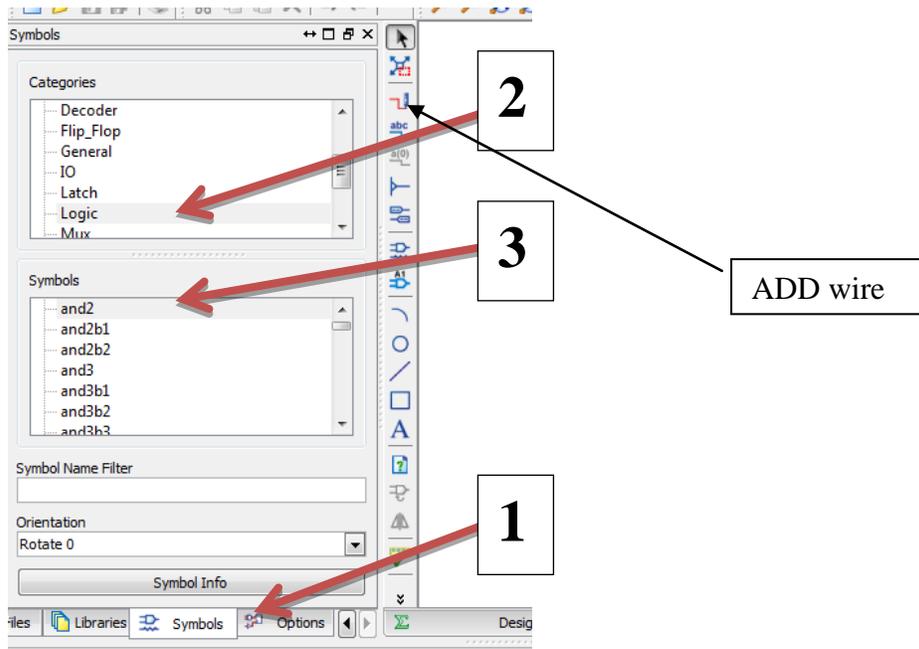
1. Open Xilinx ISE Project Navigator by double clicking the DigitalTrainer\_Simple.xise file.
2. ISE Project Navigator window will open; familiarize yourself with the project navigator: On the left there are the **Design** and **Processes** windows, and on the right there is the **Workspace**. At the bottom of the project navigator main window is the **Transcript** window.

The **Design** view window allows you to view only those source files associated with the selected View (for example, **Implementation** or **Simulation**).

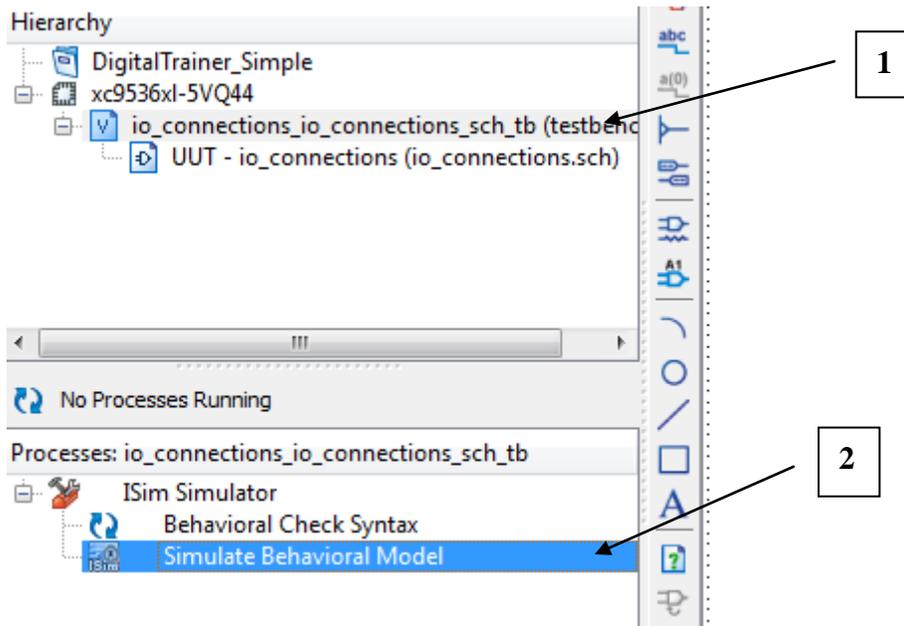
3. Select the radio button which says “Simulation” in the Design View.
4. Double-click on the ‘UUT’ (Unit Under Testing), a file named “io\_connections.sch” should open up in the Workspace.



5. Go to the 'symbols' tab, select 'Logic' as the category, and 'and2' as the Symbol:

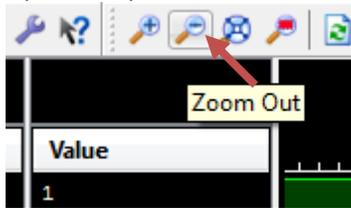


6. Place the AND gate into the blank work area of the "io\_connections.sch". You may need to zoom in, then connect up the inputs (SW1, SW2) and output (LED1) with the "ADD wire" command.
7. Save the file, then close JUST that .sch file (NOT the whole project):
8. Select 'io\_connections\_sch\_tb', then double-click 'Simulate Behavioural Model'. You may need to hit the '+' beside 'ISim Simulator':



9. In the window that opens, change to the 'Default.wcfg' tab.

10. Delete any unused signals. In this lab we only use signals SW1,SW2,LED1. Delete a signal by clicking it and hitting 'delete', or you can select a group and delete them together.
11. Use the zoom out button to get a good view of the entire waveform. You can rename the inputs/outputs to "A, B and Y" by right-clicking them and hitting 'rename'.



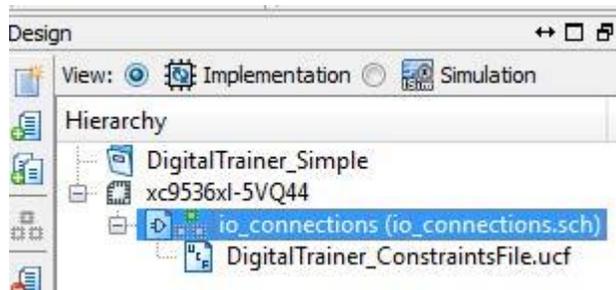
12. Using the waveform display, fill in the truth table. You may need to scroll the waveform to start at time 0 or zoom in/out. You can click on different times in the waveform and just read A/B/Y directly off. Fill in the observations based on this.

Name	Value
B	0
A	1
Y	0

13. Close the ISim window, it will ask if you really want to exit the application, hit "Yes", and "No" to save the waveform configuration.
14. Open the io\_connections.sch file again and delete the AND gate.
15. Repeat steps 5-12 with the following gates:
  - a. xor2
  - b. xnor2
  - c. nor2b1

## Part 2. Implement a 7-segment BCD Driver

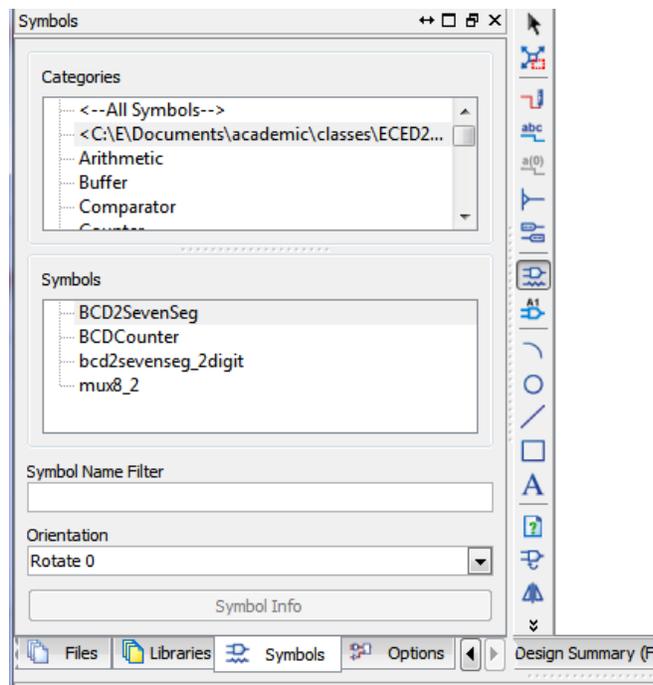
1. Select the radio button which says 'Implementation':

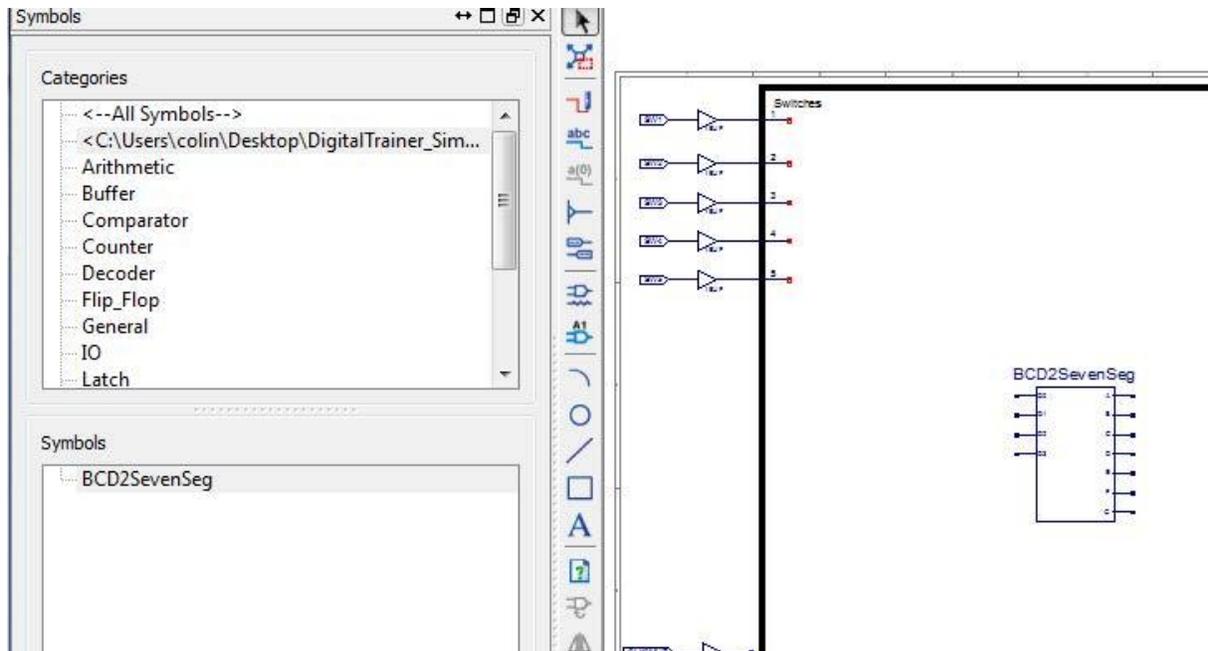


2. Open the io\_connections.sch file again and delete the logic gate if there is any.

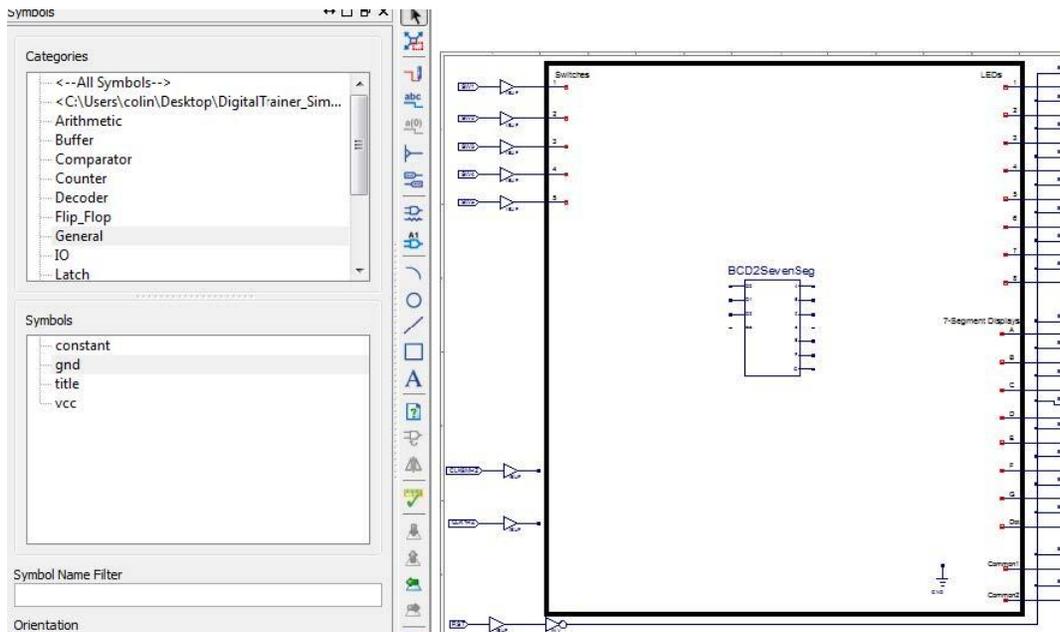
3. Place a part: 7-segment Decoder

Go to the 'Symbols' tab, and select the 2nd category on the list (will have some local path). Select 'BCD2SevenSeg', which should let you place a symbol down as the next two screen-shots show:

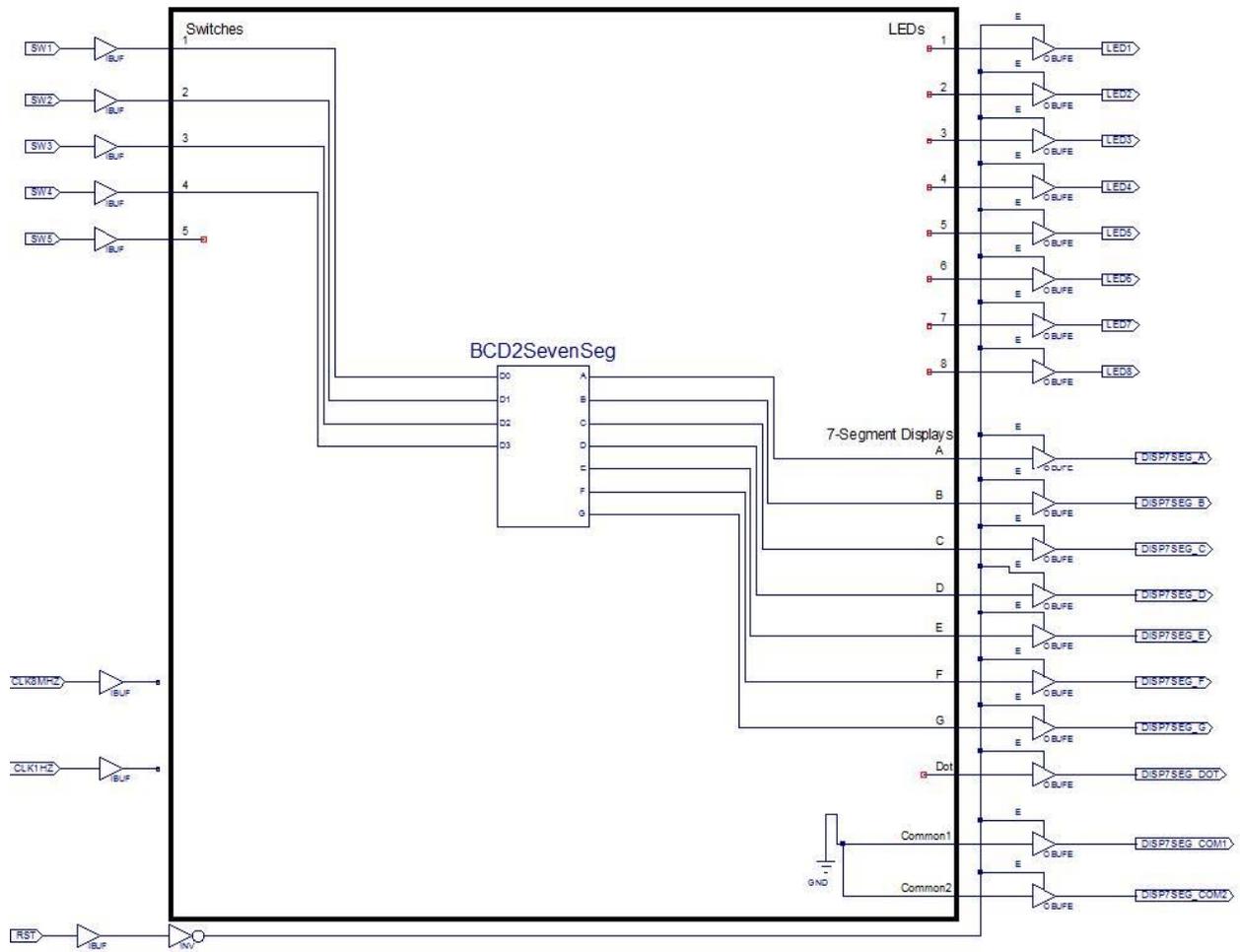




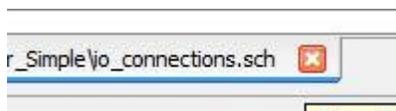
4. Place Grounds: in a similar way we need to place a GND to give the 7-segment a current sink. To do so we go to the 'general' category, and place a 'gnd' device:



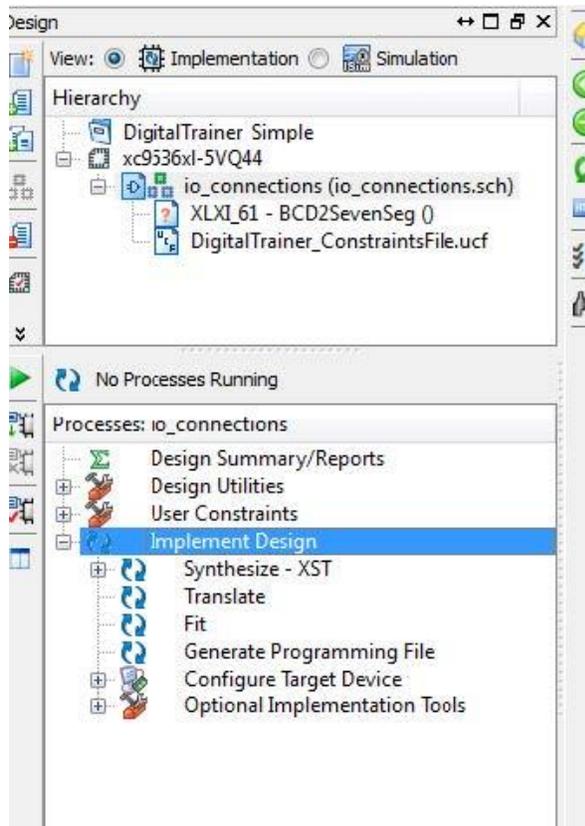
5. Wire up: using the wire tool from the toolbar, connect the 'Common1' and 'Common2' of the 7-segment displays to GND. Also connect SW1 to D0, SW2 to D1, SW3 to D2, and SW4 to D3. Finally wire up each segment of the output of the BCD2SevenSeg as in the following diagram. Note that depending on the version of your reference design it will look slightly different: don't worry about that!



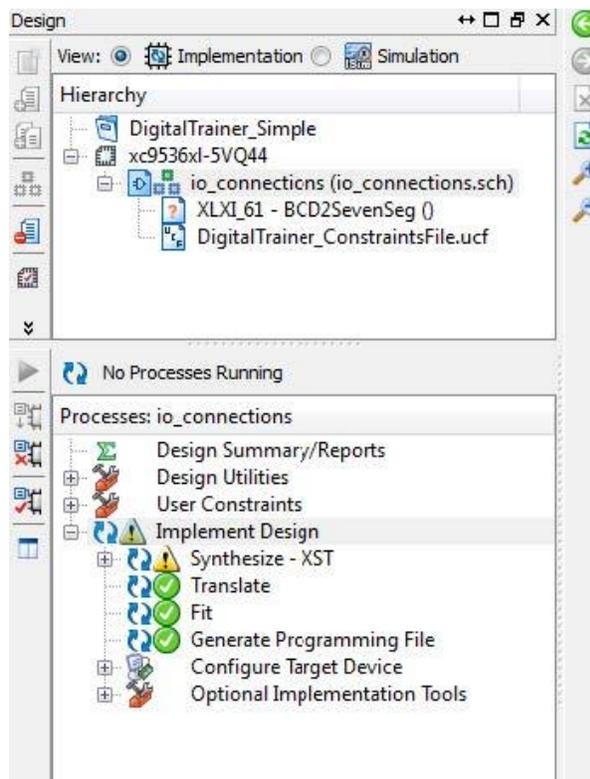
6. Save the schematic. Close that schematic file to get back to the original view:



7. Implement the design by ensuring the 'Implementation View' is still selected, then double-click on 'Implement Design':



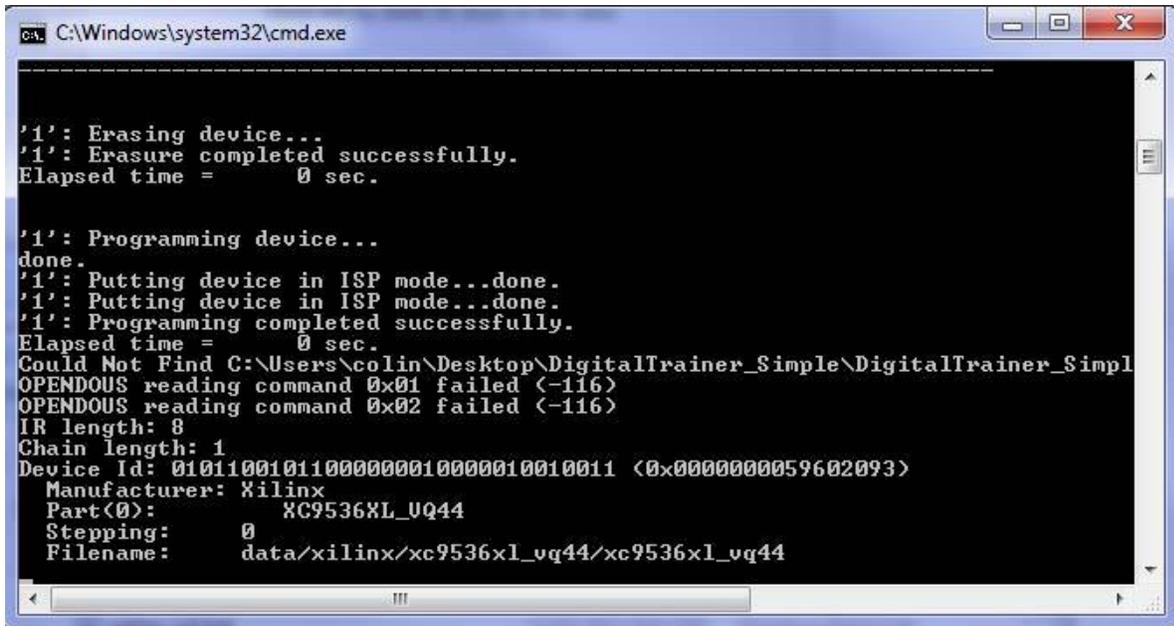
Afterwards you should get a green check-mark by 'Generate Programming File':



8. Plug in your Binary Explorer Board if you haven't already. The activity LED should illuminate briefly then go out. If it does not go out the driver install might not be finished - give it a minute, then try unplugging and re-plugging.

9. In the same folder which you opened the .xise project, find a file called either **program** or **program.bat**. Double-click this to run it:

This will open a Window, which if successful takes about 30-60 seconds to run.

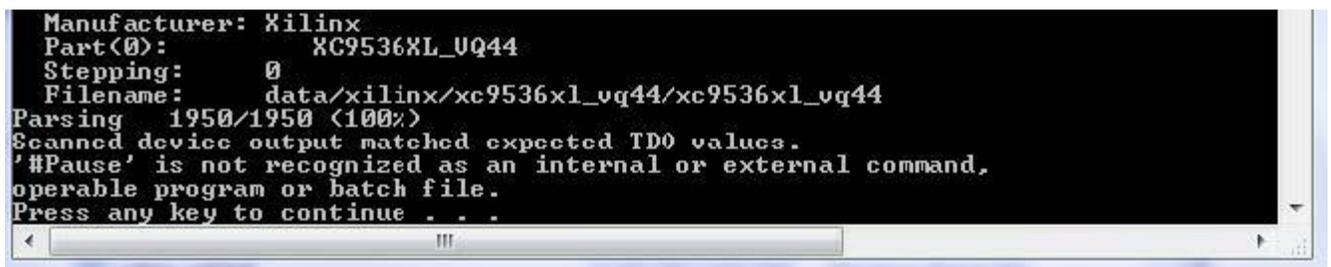


```
C:\Windows\system32\cmd.exe

'1': Erasing device...
'1': Erasure completed successfully.
Elapsed time =      0 sec.

'1': Programming device...
done.
'1': Putting device in ISP mode...done.
'1': Putting device in ISP mode...done.
'1': Programming completed successfully.
Elapsed time =      0 sec.
Could Not Find C:\Users\colin\Desktop\DigitalTrainer_Simple\DigitalTrainer_Simpl
OPENDOUS reading command 0x01 failed (-116)
OPENDOUS reading command 0x02 failed (-116)
IR length: 8
Chain length: 1
Device Id: 01011001011000000010000010010011 <0x0000000059602093>
Manufacturer: Xilinx
Part(0):      XC9536XL_UQ44
Stepping:     0
Filename:     data/xilinx/xc9536x1_uq44/xc9536x1_uq44
```

10. If the download is successful you will see the line "Scanned device output matched expected TDO values". You can press enter to exit the programming script.



```
Manufacturer: Xilinx
Part(0):      XC9536XL_UQ44
Stepping:     0
Filename:     data/xilinx/xc9536x1_uq44/xc9536x1_uq44
Parsing      1950/1950 <100%>
Scanned device output matched expected TDO values.
'#Pause' is not recognized as an internal or external command,
operable program or batch file.
Press any key to continue . . .
```

11. Once the program is downloaded, make sure the 'CPLD Reset' switch is set to 0 (towards bottom), and try varying the inputs to see how the 7-segment display varies. Fill out the observation form.

## Digital Circuits - ECED 2200 Tutorial 1 Observations

Student Names: \_\_\_\_\_ B00 \_\_\_\_\_  
 \_\_\_\_\_ B00 \_\_\_\_\_

**AND2 Gate Truth Table:**

A	B	Y
0	0	
0	1	
1	0	
1	1	

**XNOR2 Gate Truth Table:**

A	B	Y
0	0	
0	1	
1	0	
1	1	

**XOR2 Gate Truth Table:**

A	B	Y
0	0	
0	1	
1	0	
1	1	

**NOR2B1 Gate Truth Table:**

A	B	Y
0	0	
0	1	
1	0	
1	1	

### Part 2. Implement a 7-segment BCD Driver

Switches $SW_3 SW_2 SW_1 SW_0$	Display (color the light-up segments)
0 0 0 0	
0 0 0 1	
0 0 1 0	
0 0 1 1	
0 1 0 0	
0 1 0 1	
0 1 1 0	
0 1 1 1	
1 0 0 0	
1 0 0 1	
1 0 1 0 – 1 1 1 1	Don't Cares