Assignment #1 – ECED 4260

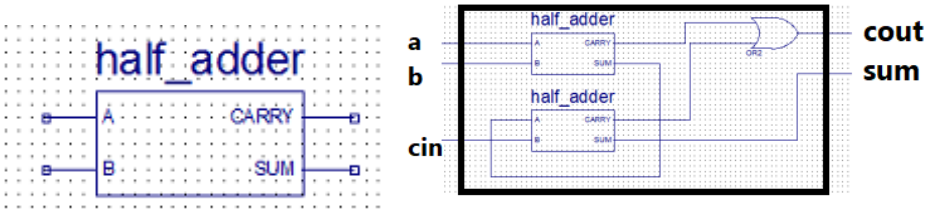
Note: Please include headers for the HDL code. Two example headers are provided below.

```
-------------------------------------------------
-- Assignment 1. 4:1 Multiplexer
-- Author:       ECED 4260
-- Student ID:   B00-------
-- Date:         September xx, 2024
-- File Name:    light.vhd
-- Architecture: Structural with 2:1 MUX
-- Description: …..
-- Acknowledgements:
-------------------------------------------------
```

```
/*
A two-way light controller
Author:       ECED 4260
Student ID:   B00-------
Date:   September xx, 2024
File Name:    light.v
Description: The circuit can be used to….
Acknowledgements:
*/
```

1. Build an HDL model of a 4-to-1 Multiplexer using 2-to-1 Multiplexer as components.

2. Design a Half Adder using VHDL or Verilog, and use it to build a Full Adder.



3. Design a Binary Coded Decimal (BCD) – to - 7-segment display decoder using VHDL or Verilog. The seven outputs of the decoder, ***a*** to ***g***, are active high (i.e. a '1' will light up the corresponding segment).

4. Build a finite state machine that detects the patterns of "1001" and "1101" from a serial bit stream, overlapping allowed. When the state machine detects the pattern, it will set its output signal to '1' for a clock cycle.
(a) Draw the state transition diagram. Label all nodes and arcs.
(b) Derive the next state logic and the output logic equations.
(c) Write an HDL model of this FSM.
(d) Use ModelSim to simulate your pattern detector, and attach a screenshot of your simulation result.