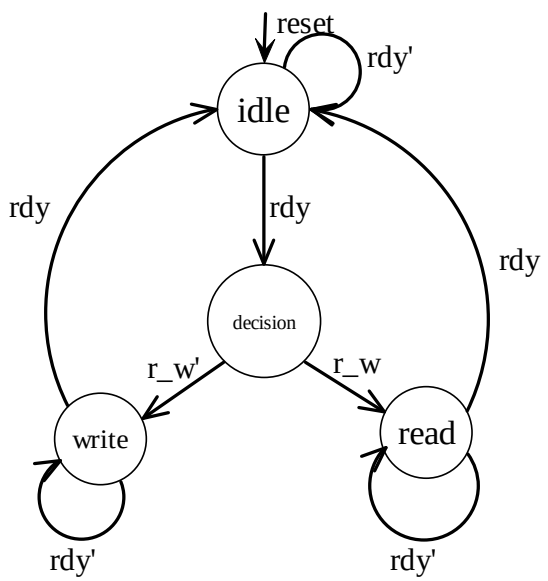
Assignment #2 – ECED 4260

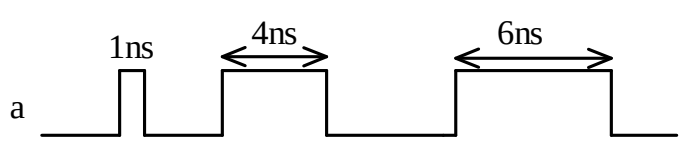
1. A finite state machine is shown below, and the output table is provided. Write an HDL model of this state machine.

State	Outputs	
	Oe	We
Idle	0	0
Decision	0	0
Write	0	1
Read	1	0



2. Draw a timing diagram which illustrate the difference between the following VHDL statements

Signal a, b, c, d: bit;
B <= a after 5 ns;
C <= transport a after 5 ns;
D <= reject 3ns inertial a after 5 ns;



3. Build an HDL model of a 4-to-1 Multiplexer using 2-to-1 Multiplexer as components. Sample VHDL codes of Multiplexers can be found at http://mems.ece.dal.ca/eced4260/lab1.htm (part I and II).

4. Consider the design of a Moore FSM with a 1-bit input (I), and a 1-bit output (O). The FSM accepts inputs one bit at a time and outputs a 0 until it sees the sequence 0101 (with no other bit values in between). After seeing the 0101 sequence it outputs a 1 and then starts over again.
(a) Draw the state transition diagram. Label all nodes and arcs.
(b) Derive the next state logic and the output logic equations.
(c) Write an HDL model of this FSM.

5. Build a finite state machine that detects the overlapping patterns of “11001” and “1101” from a serial bit stream. When the state machine detects the pattern, it will set its output signal to ‘1’ for a clock cycle. For this, you will need to demonstrate a state diagram, state reduction table, Karnaugh maps and equations for implementation with D flip-flops.