Assignment #1 - ECED 4260 IC Design and Fabrication

1) Simplify the following functions using the theorems of Boolean algebra. F1(X,Y,Z)=YZ'+X'YZ+XYZ ; F2(X,Y,Z)=(X+Y)(X'+Y+Z)(X'+Y+Z'); F3(W,X,Y,Z)=X+XYZ+X'YZ+X'Y+WX+W'X
2) Design a mealy sequential circuit with one input and one output which detects instances of the patterns "101" and "001", including overlapping patterns.
3) A finite state machine has one input and one output. The output becomes 1 and remains 1 thereafter when at least two 0's and at least two 1's have occurred as inputs, regardless of the order of occurrence. Assuming this is to be implemented as a moore machine, draw a state diagram.
4) Reduce the number of states in the following state table to the minimum number required.

Present State	Next state		Output
	Input X=0	Input X=1	
S0	S5	S2	0
S1	S3	S5	0
S2	S7	S0	0
S3	S1	S6	0
S4	S6	S5	1
S5	S0	S6	0
S6	S4	S7	1
S7	S2	S4	0

5) Which of the following are valid VHDL basic identifiers? Which are reserved words?
Not_bad not good 1word srl _score
This_is_one #5_isnot How_about_this_one Last_one
6) Write entities and architectures, which describe the circuits shown below. For the first one, just use Boolean algebra. For the second one, you are required to construct a two input and gate and use component instantiation to build the three input and gate.