Department of Electrical & Computer Engineering
Dalhousie University

ECED 4260
IC Design and Fabrication
Midterm Examination

Instructor:	Y. Ma
Exam date:	Oct. 31, 2017
Exam duration:	80 minutes
Aids permitted:	This is a closed book exam. No books or notes are to be consulted. Two double-sided 8.5″x11″ formula sheets are allowed.

Instructions:
1. Provide your name printed, signature and I.D. number on this page.
2. Verify that this booklet contains 7 pages (including the cover page).
3. Neatly enter your answers in the spaces provided.
4. Use the reverse sides of the pages for rough work.

Student name: _____

Signature: _____

Student ID: _____

Reference Solution

Question	Time (min)	Worth	Mark	Subject
1	15	10		Multiple Choice Questions
2	15	15		Logic Simulation
3	15	15		VHDL
4	25	25		Finite State Machine
Total	70 min	65		

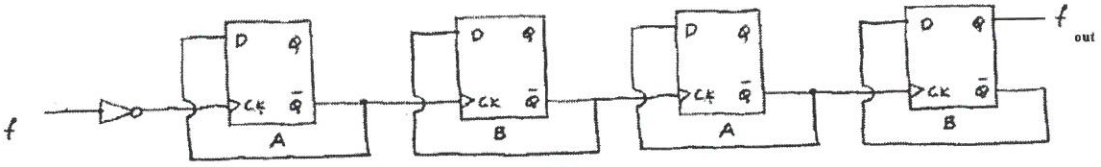
Q1. Multiple-choice questions. Circle **ONLY ONE** that apply. [1 pt each]

(1) VHDL stands for

(a) Very Hard Detailed Language (b) Variable Hierachy Discussion Language

(c) VHSIC Hardware Description Language

(2) Four (4) D flip-flops are connected in tandem as a Frequency Divider. For a 2 MHz square wave input frequency, determine the frequency of the output:



(a) 1MHz (b) 500 kHz (c) 125 kHz (d) None of the above

(3) To implement a T flip-flop using a JK flip-flop:

(a) J=K=1 (b) J=T, K=0 (c) J=T, K=T' (d) J=K=T

(4) Synchronous digital logic means:

(a) All gates are triggered at the same time (b) All Flip-Flops are triggered at the same time (c) All events occur at the same time

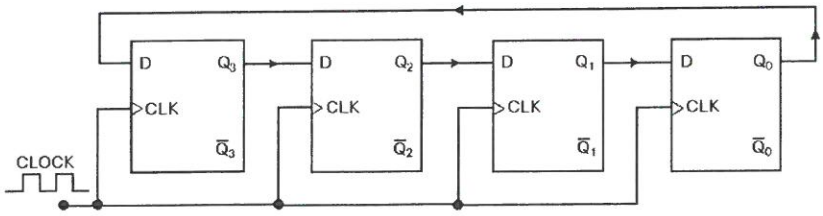
(5) A maximum length linear feedback shift register (LFSR) of four Flip-Flops has how many states:

(a) 4 (b) 8 (c) 15 (d) 16

(6) The bit sequence 0010 is serially entered (right-most bit first) into a 4-bit parallel out shift register that is initially clear. What are the Q outputs after two clock pulses?

(a) 1000 (b) 0010 (c) 0000 (d) 0001

(7) For a 4-bit ring counter as shown below, one of the FFs is preset with a 1 and all others are cleared to 0s. How many states does this ring counter have?



(a) 4 (b) 8 (c) 15 (d) 16

(8) If we add an inverter to the feedback path of the above ring counter, we have a Johnson counter.

On the fifth clock pulse, a 4-bit Johnson counter sequence is Q_3= 0, Q_2=1, Q_1=1, Q_0=1.

On the sixth clock pulse, the Q_3Q_2 Q_1 Q_0 sequence is _____.

(a) 1011 (b) 1000 (c) 0011 (d) 0001

(9) How many flip-flops are necessary to design a state machine with 25 states?

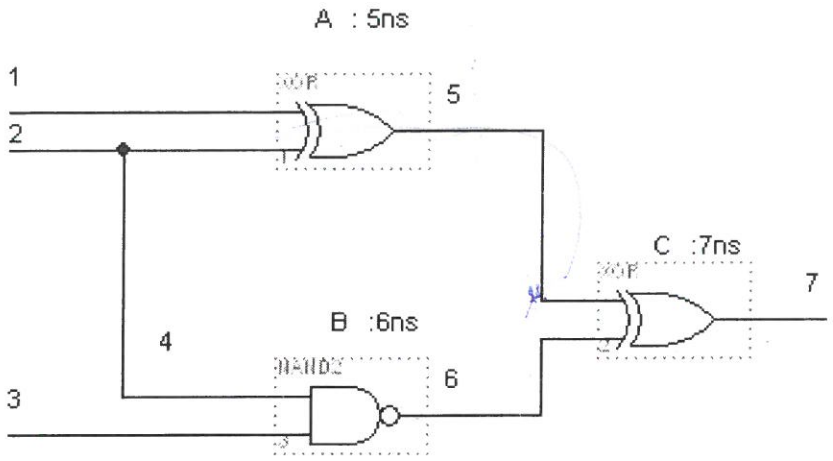
(a) 4 (b) 5 (c) 25 (d) 2^{25}

(10) Which type of finite state machines has outputs that will only change on the edge of a clock pulse?

(a) Moore (b) Mealy (c) Mealy-Moore (d) None of the above

Question 2. (15 marks)

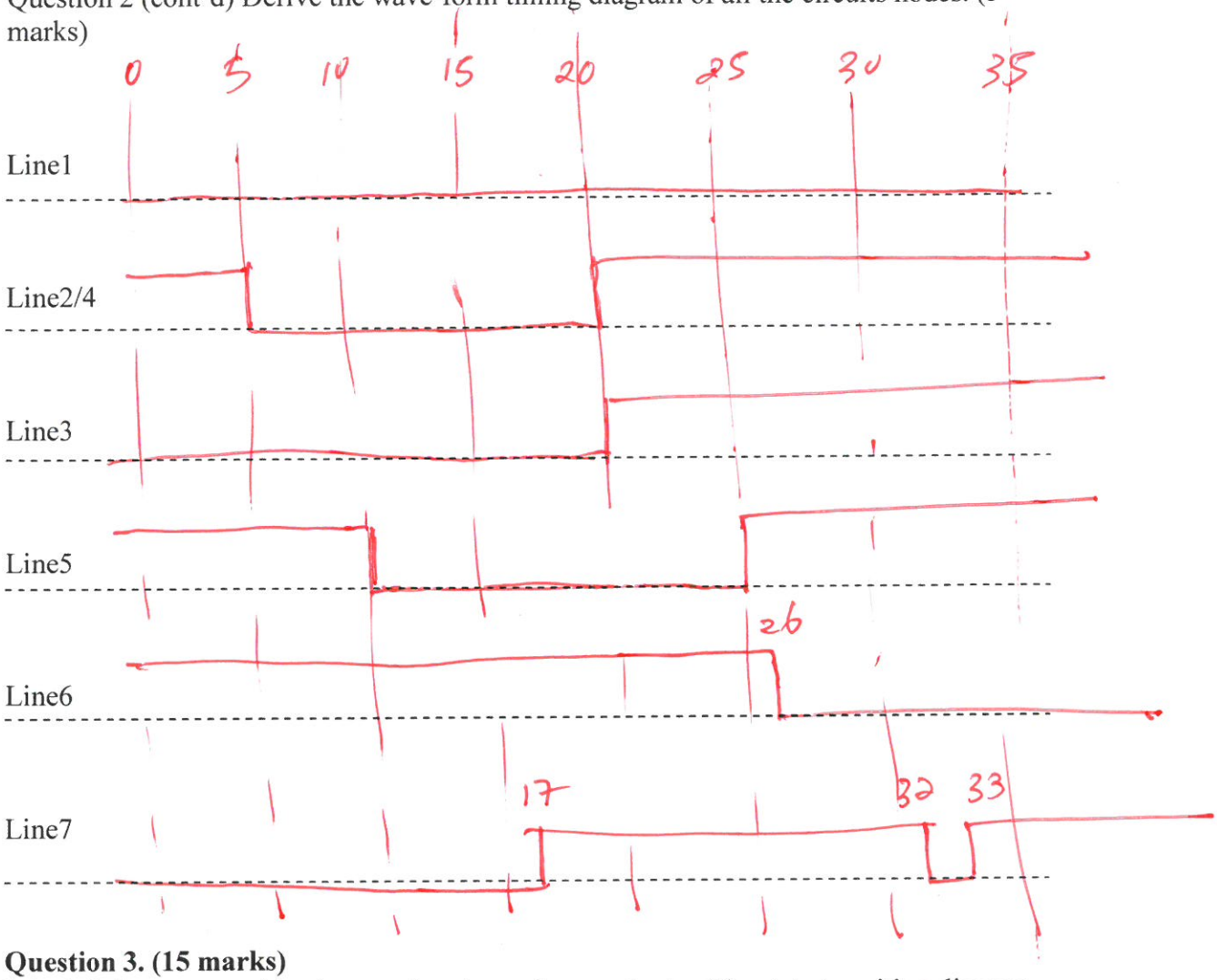
The circuit given below has been initialized by input Line**1** Line**2** Line**3** = 010 and all the circuit nodes are in known stable states. Perform the event-driven simulation of the circuit for two input vectors Line**1** Line**2** Line**3** = 000 at **t = 5 ns**, and Line**1** Line**2** Line**3** = 011 at **t = 20 ns**, following the initialization.



2.1 Complete the simulation table below (10 marks)

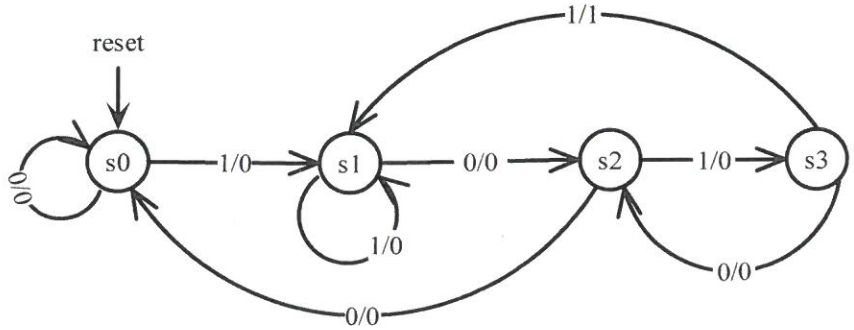
	Line values							Gates affected			Scheduled events
Time	1	2	3	4	5	6	7	A	B	C	
0ns	0	1	0	1	1	1	0				
5		0		0				X	X		(5, 0) @ 10
10					0					X	(7, 1) @ 17
17							1				
20		1	1	1				X	X		(5, 1) @ 25
											(6, 0) @ 26
25					1				\	X	(7, 0) @ 32
26						0				X	(7, 1) @ 33
32							0				
33							1				

Question 2 (cont'd) Derive the wave-form timing diagram of all the circuits nodes. (5 marks)



Question 3. (15 marks)

3.1 A finite state machine has one input x and one output z. The state transition diagram is shown below. Explain what the machine is supposed to do. (5 marks)



Your Answer: Detec "1011" overlapping permitted

/ Set z high for 1 clock period when "1011" detected

3.2 The VHDL code given below describes the above FSM with an extra output showing the binary assignment of the states.
(a) (5 marks) By writing directly in the code, show how to add Mealey output z to the state machine. Label these changes with (a).
(b) (5 marks) By writing directly in the code, indicate how an asynchronous reset can be added that causes transitions to the state s0. Label these changes with (b).

```
library ieee;
use ieee.std_logic_1164.all;

entity example is
        port (clk: in std_logic;
                x: in std_logic;
                stateout: out std_logic_vector (1 downto 0));
end entity example;

architecture state_machine of example is
        type statetype is (s0, s1, s2, s3);
        signal present_state, next_state: statetype;
begin
        comb_logic: process (present_state, x) begin
                Case present_state is
                        when s0 => stateout<="00";
                                If (x='1') then next_state<=s1;
                                else next_state<=s0;
                                end if;
                        when s1 => stateout<="01";
                                If (x='0') then next_state<=s2;
                                else next_state<=s1;
                                end if;
                        when s2 => stateout<="10";
                                If (x='1') then next_state<=s3;
                                else next_state<=s0;
                                end if;
                        when s3 => stateout<="11";
                                If (x='1') then next_state<=s1;
                                else next_state<=s2;
                                end if;
                end case;
        end process comb_logic;

        memory_element: process (clk) begin
                If (clk'event and clk='1') then
                present_state <= next_state;
                end if;
        end process memory_element;

end architecture state_machine;
```

, reset (b)

z : out std_logic); (a)

z <= '0'; z <= '0'; z <= '0'; z <= '0'; z <= '0'; z <= '0'; z <= '1'; z <= '0'; (a)

reset

elsif

If (reset = '1') then present_state <= S0;

(b)

Question 4. (25 marks) Finite State Machine

4.1 (5 marks) By writing directly in the code, correct 6 errors which would be detected by a VHDL compiler. Label the corrections.

```
-- some kind of finite state machines --
entity ever is
        port (clock, X: in bit;
                A, B, done: out bit);
end ever;

architecture what of ever is
signal next_A, next_B: bit;

begin
Next_A<=    (not A and not B and X) or (not A and B and not X) or (A and B and X) or
            (A and not B and not X) ;
Next_B<=    (not A and not B) or (A and not B);
Done<=      (A and B and not X) or (A and B and X);

state: process (clock)
begin
   if clock'event and clock='1' then
   B<- next_B;
   A<- next_A;
   endif;
end process ever;
end what;
```

inout

$\bar{A}\cdot\bar{B}\cdot X + \bar{A}\cdot B\cdot\bar{X} + ABX +$

$A\cdot\bar{B}\cdot\bar{X}$

$\bar{A}\cdot\bar{B} + A\cdot\bar{B}$

$A\cdot B\cdot\bar{X} + A\cdot B\cdot X$

<= <= state

4.2 (5 marks) Fill the K-maps and write the **simplest** Boolean expressions for **next_A, next_B**, and **done**.

Next_A		A B			
		00	01	11	10
X	0		1		1
	1	1		1	

Next_A = $A \oplus B \oplus X$

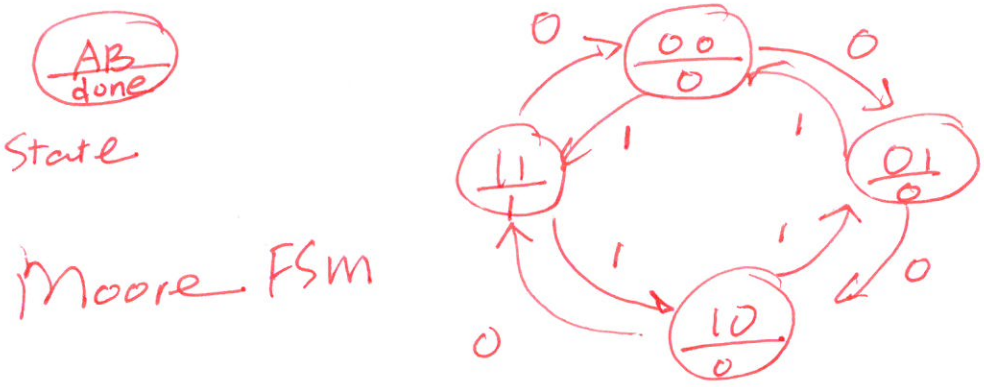
Next_B		A B			
		00	01	11	10
X	0	1			1
	1	1			1

Next_B = $\bar{B}$

done		A B			
		00	01	11	10
X	0			1	
	1			1	

done = $A\cdot B$

4.3 (5 marks) Draw a state transition graph (with outputs) for this finite state machine. Is this a Moore machine or a Mealy machine?



4.4 (10 marks) Use JK flip-flops to implement this Finite State Machine: Find minimized logic for the inputs of JK flip-flops, and draw the resulting circuit that implements this FSM.