ECED 4260

Part I Review of Classical Sequential Logic Design
Must-Knows

The must-knows of part I are outlined but not limited to the followings:

- Boolean algebra
- Karnaugh maps, minimum S.O.P, minimum P.O.S.
- Memory elements
- FSM, design of Mealy and Moore machine
- PLAs

Part II VHDL & Simulation
Must-Knows

The must-knows of part II are outlined but not limited to the followings:

- Classes of objects (constants, variables and signals)
- Object types (scalar and composite)
- Modes (in, out, inout, buffer)
- Design units
- Modeling of concurrency
    - processes
    - concurrent and sequential statements
- Modeling of circuits' behavior, structure and timing, process implementation of FSMs, decoders, etc.
- Miscellaneous
    - given a simple combinational circuit
        derive the simulation table
        construct event lists
        derive the timing diagram of the circuit from the simulation table