ECED 4260 Must-Knows

Part III Digital Design & Applications

The must-knows of part III are outlined but not limited to the followings:

- Using Variable Entered Maps for logic minimization
- Using state diagram to describe the behavior of a digital system
- Design procedures for synchronous digital systems:
    - Given a problem statement, define the digital system specifications
    - Derive a rough flowchart and block diagrams from the system specs
    - Develop the detailed flowchart and design the complete datapath
        - be familiar with the register-transfer level logic devices
    - Complete the design of the controller
        - using D/JK FF to implement the state variables

Part IV Design of Arithmetic Circuits

The must-knows of part IV are outlined but not limited to the followings:

- Converting numbers to different radix representation
- Representing negative numbers using signed magnitude, 1's and 2's complement
- Two's complement addition and subtraction
- Design of fast adder using carry look ahead (CLA)
- Design idea of CLA and CLG
- Critical path / worst delay of different adder design
- Booth re-coded multiplier and modified Booth fast multiplier
- Binary division using restoring/non restoring comparison method
- IEEE 754 floating point numbers
- Floating point addition and multiplication

Part V Digital System Testing

The must-knows of part III are outlined but not limited to the followings:

- Single stuck-at fault model (gate level)
- Detectable and undetectable faults
- Fault collapsing
- Automatic test pattern generation for deterministic testing
    - Given a gate-level circuit scheme with s line segments
        - Find all equivalent faults and form the reduced fault set of k faults
        - Find a test vector for a given single stuck-at fault
        - Find the minimal test set for the k faults
- Signature analysis
    - Given a polynomial P(x), determine its primitivity by checking if the pseudo-random sequence generated has the maximum length cycle

    - Given a polynomial P(x), draw the corresponding LFSRs for PTPG and data compaction
    - Given a circuit and a degree n polynomial
        - Derive the test sequence generated by the LFSR
        - Determine the fault free signature of the circuit
        - Compute the signature of the fault circuit responses
        - Determine if the fault is detectable by the test set
- Testing architectures for industrial circuits
    - scan-based test
    - IEEE standard 1149.1 (also called the boundary scan standard)