ECED 4260 IC Design and Fabrication

Tutorial D: Timing Analyzer

Tutorial Material:

- Download the **add_three_numbers.vhd or .v** to your work directory.
- Follow Intel Tutorial: **Using the Timing Analyzer**

Submissions after the tutorial:

- A summary of what you have leant from this tutorial
- The HDL file including your names and Banner numbers
- The clock constraint (.sdc) file created as shown in section 4.1
- The summary of paths, the path summary of path 1 and the waveform of path 1 for all 3-timing analysis: the violated analysis, the regenerated analysis, and the analysis with the created clock. All three windows are shown in Figure 7 and can be undocked and screenshotted.
- Finally, a brief explanation of slack, clock skew, and worst-case delay and calculations of those 3 values for the timing analysis with the created clock.

All of these are to be put in a pdf document, no formal report is required. A suggested template can be found on the next page.

Name

B00

Date

ECED4260

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Summary

Part 1

[Screenshots]

Part2

[Screenshots]

Part3

[Screenshots]

Equations and Descriptions

Code

[Vhd and sdc file]