Department of Electrical & Computer Engineering
Dalhousie University

ECED 4260
IC Design and Fabrication
Final Examination

Instructor: Y. Ma
Exam date: Dec. 6, 2006
Exam duration: 180 minutes
Aids permitted: This is a closed book exam. No books or notes are to be consulted. Three double-sided 8.5"x11" formula sheets are allowed.

Instructions:
1. Provide your name printed, signature and I.D. number on this page.
2. Verify that this booklet contains 9 pages (including the cover page).
3. Neatly enter your answers in the spaces provided.
4. Use the reverse sides of the pages for rough work.

Student name: Reference Solution

Signature: _____

Student ID: _____

Question	Time (min)	Worth	Mark	Subject
1	40	25		VDHL, Combinational logic
2	30	10		Design of Fast Adder
3	15	8		Booth Multiplication
4	25	12		Floating Point Numbers
5	40	30		Digital System Testing
6	30	15		IC Fabrication
Total	180 min	100		

Question 1. (20 marks)

1.1 (6 marks) By writing directly in the code, correct 6 errors which would be detected by a VHDL compiler. Label the corrections.

```
-- some kind of finite state machines --
entity ever is
        port (clock, clear, enable: in bit;
              y1, y0, done: out bit);
end ever;

architecture what of ever is
signal next_y1, next_y0: bit;

begin
next_y1<= ((y1 and not y0 and not enable) or
      (y1 and y0) or (not y1 and y0 and enable)) and not clear;
next_y0<= (not y1 and enable) or (not y1 and y0) or (y0 and not enable) or clear;
done<= y1 and not y0;

state: process (clock)
begin
   if clock'event and clock='1' then
   y1<= next_y1;
   y0<= next_y0;
   endif;
end process ever;
end what;
```

① ② inout ③ ④ ⑤ end if; ⑥ state

$y_1 \cdot \bar{y}_0 \cdot \bar{en} + y_1 \cdot y_0 + \bar{y}_1 \cdot y_0 \cdot en + \bar{cl}$

$\bar{y}_1 \cdot en + \bar{y}_1 \cdot y_0 + y_0 \cdot \bar{en} + cl$

1.2 (6 marks) Create minimal sum-of-product expressions for next_y1, next_y0 and done.

Next_y1		y1,y0 =			
		00	01	11	10
clear,enable=	00			1	1
	01		1	1	
	11				
	10				

Next_y1 = $y_1 \bar{en} \cdot \bar{cl} + y_0 \cdot en \cdot \bar{cl}$

2/5

Next_y0		y1,y0 =			
		00	01	11	10
clear,enable=	00			1	
	01				
	11	1	1	1	1
	10	1	1	1	1

Next_y0 = $clear + y_0 \cdot \bar{en} + \bar{y}_1 \, en$

2/5

if clear = 1 next_y0 = 1 next_y1 = 0

01

$y_1 y_0$ \ $y_1^+ y_0^+$	00	01	11	10
00	00	01		
01	01	11		
11	11	10		
10	10	00		

$cl \cdot en$

4/5

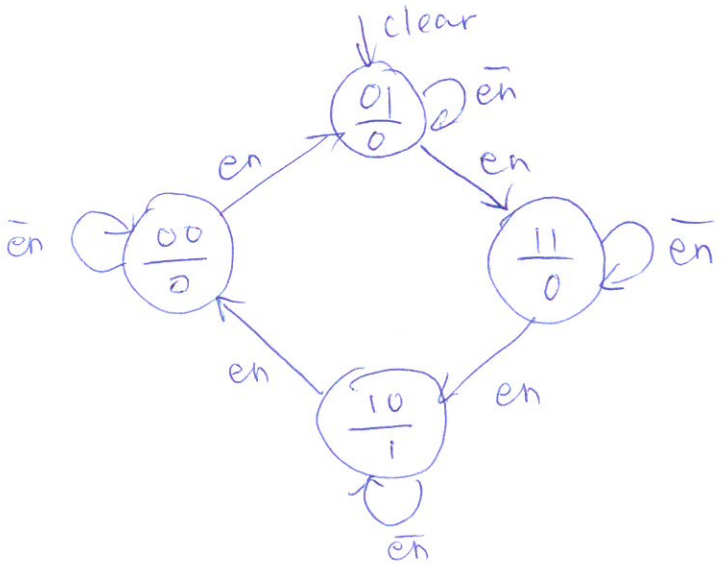
done		y1,y0 =			
		00	01	11	10
clear,enable=	00				1
	01				1
	11				1
	10				1

done = $\bar{y}_0 y_1$

1.3 (6 marks) Trace the execution of the VHDL code (with the reasonable corrections made). Assume that enable and clear have settled before any clock edge. Fill in the values that the signals would take on after they become stable following any clock edge.

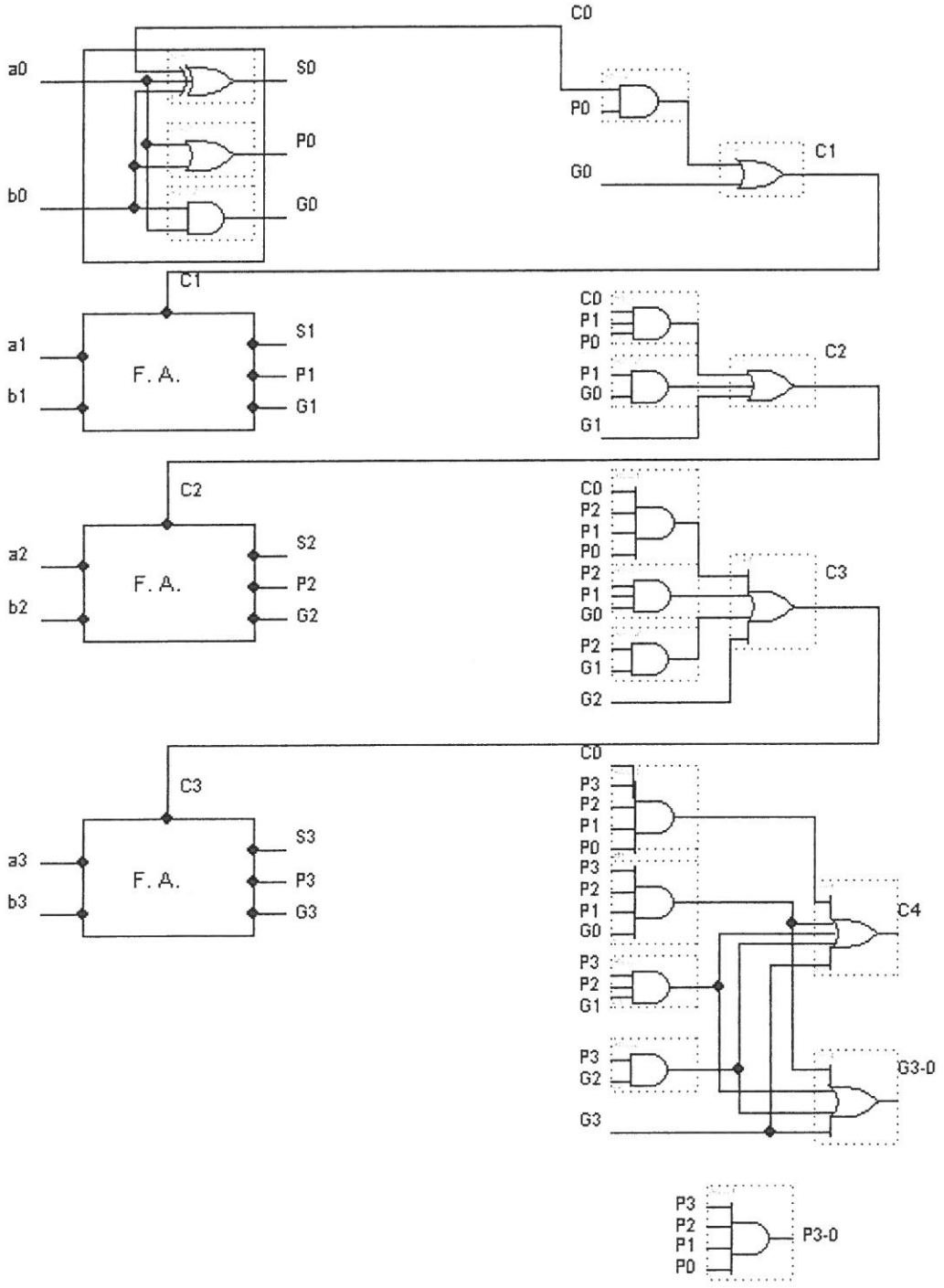
enable	clear	clock	next_y1	next_y0	y1	y0	done
0	0	1	0	0	0	0	0
0	1	↓	0	1	0	0	0
1	1	0	0	1	0	0	0
1	0	↑	1	1	0	1	0
1	0	1	1	1	0	1	0
→ 1	1	↓	0	1	0	1	0
→ 1	0	↑	1	0	[illegible]	1	0
0	0	↑	1	1	1	1	0
1	1	↑	0	1	0	1	0
1	0	↑	1	0	1	1	0
1	0	↑	0	0	1	0	1
1	0	↑	0	1	0	0	0
1	0	↑	1	1	0	1	0

1.4 (4 marks) Draw a state transition graph for the finite state machine.



Question 2. (10 marks)

2.1. (5 marks) Observe the structural regularity of the 4-bit carry look-ahead (CLA) adder circuit given and derive the sum-of-product expressions of a 6-bit CLA adder for C4, C5, C6, P5-0 and G5-0 in terms of C0, P0, P1, …, P5, G0, …, and G5. Identify the critical path of the 6-bit CLA adder. How much time does it take to add two 6-bit binary numbers (i.e. the worst case delay)?



C4 = $G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_0$

/2 C5 = $G_4 + P_4G_3 + P_4P_3G_2 + P_4P_3P_2G_1 + P_4P_3P_2P_1G_0 + P_4P_3P_2P_1P_0C_0$

C6 = $G_5 + P_5G_4 + P_5P_4G_3 + P_5P_4P_3G_2 + P_5P_4P_3P_2G_1 + P_5P_4P_3P_2P_1G_0 + P_5P_4P_3P_2P_1P_0C_0$

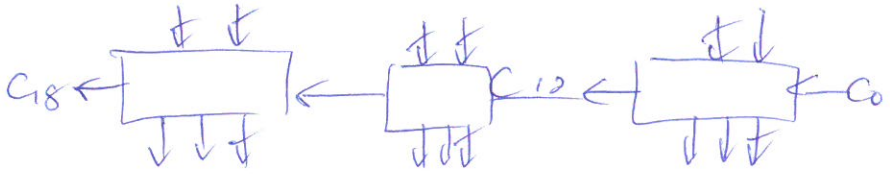
P5-0 = $P_5P_4P_3P_2P_1P_0$

G5-0 = $G_5 + P_5G_4 + P_5P_4G_3 + P_5P_4P_3G_2 + P_5P_4P_3P_2G_1 + P_5P_4P_3P_2P_1G_0$

/3 The critical path is $C_0 \rightarrow C_5$, $(a_i/b_i/c_0 \rightarrow S_i)\ C_5 \rightarrow S_5$

The worst case delay = $3\tau_g + 3\tau_g = 6\tau_g$

2.2 (5 marks) What is the worst case delay for three cascaded 6-bit CLAs to add together two 18-bit binary numbers?



$C_0 \rightarrow C_6$	$3\tau_g$
$C_6 \rightarrow C_{12}$	$2\tau_g$
$C_{12} \rightarrow C_{17}$	$2\tau_g$
$C_{17} \rightarrow S_{17}$	$3\tau_g$

$10\tau_g$

Question 3. (8 marks)

3. Multiply the following pairs of two's complement notation numbers using Booth multiplication for the first problem and fast multiplication (modified Booth algorithm) for the second problem. Show all partial products in the spaces provided.

			1	0	1
			1	1	0
			0	-1	0
					0
		0	1	1	
			0		
0	0	0	1	1	0

$m^* = 011$

Re-code 1 per code

					1	1	0	1
			1	1	1	0	1	0
				0		-1		-2
					0	1	1	0
			0	0	1	1		
				0				
			0	1	0	0	1	0

$m^* = 0011$

$2m^* = 0110$

Question 4. (12 marks)

4.1 (6 marks) Determine the single precision representation of 39.0625×10^{-3}.

→ Exp 1.5

0	0	1	1	1	1	0	1	0	0	1	0																			0

$39.0625 \times 10^{-3} = 0.0390625 \times 2^5 = 1.25$ 1

$0.25 \times 2 = 0.5$ 0

$0.5 \times 2 = 1$ 1

$\therefore 39.0625 \times 10^{-3} = 1.01 \times 2^{-5}$

$127 - 5 = 122$

4.2 (6 marks) Add the following two numbers, which are given in IEEE 754 notation.

2^2

2^4

0	1	0	0	0	0	0	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

shift 6 →

2^{-4} 0 0 0 0 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0

0	0	1	1	1	1	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	0	0	0	1	0	

2^{-2}

→

0	1	0	0	0	0	0	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1	1

Result = $1.101011\cdots1 \times 2^2$

$= 110.1011\cdots1$

$= 6 + 2^{-1} + 2^{-2} - 2^{-23}$

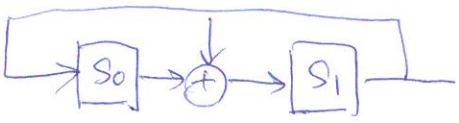
$\doteq 6.75$

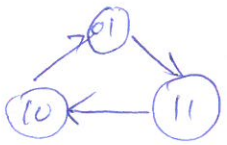
$26.\ 2^{-1} + 2^{-2} - 2^{-23}$

Question 5. (30 marks)
Design a test pattern generator using an autonomous linear feedback shift register and determine if it can test the circuit provided.

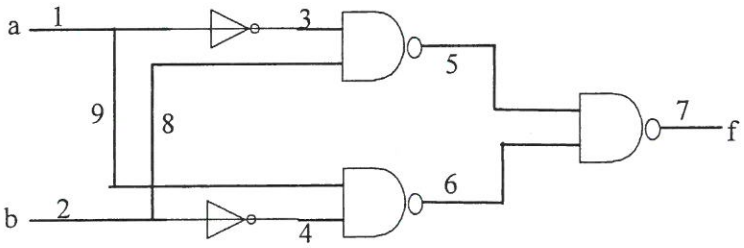
5.1 (7 marks) Create a degree-2 primitive polynomial P(x). Provide the polynomial, the corresponding circuit diagram of the ALFSR and a state transition graph.

$P(x) = x^2+x+1$





5.2 (18 marks) Using the stuck at model for following circuit, find out one test vector for every stuck at fault on a labeled wire. Provide the input (a,b), correct output (f) and faulty output (f*). You may wish to list additional test vectors outside the table.



Wire	Stuck at 0 abff*	Stuck at 1 abff*
1	1010 / 1101	0001 / 0110
2	0110 / 1101	0001 / 1010
3	01 10	11 01
4	10 10	11 01
5	00 / 11 01	01 10
6	00 / 11 01	10 10
7	1010 0110	00 / 11 01
8	01 00	00 01
9	1010	00 01

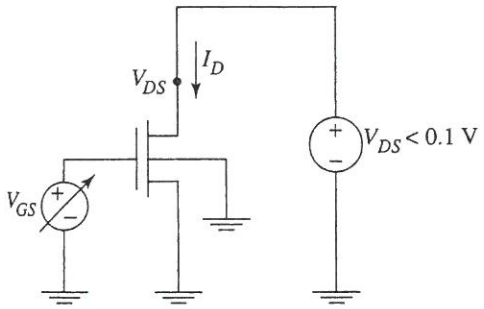
5.3 (5 marks) What is the minimum test pattern required? Can the ALFSR you designed produce all of the required test patterns?

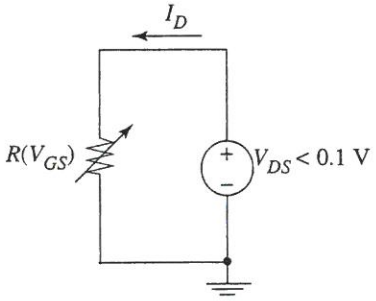
(4) 01, 10, 11, 00

No.

Question 6. (15 marks)

6.1 (8 marks) The circuit below shows an n-channel MOSFET that is used as a voltage-controlled resistor. A MOSFET in this configuration is found in circuits such as variable gain amplifiers. Find the sheet resistance of the MOSFET ($R_\square$) over the range $V_{GS} = 1.5V$ to $V_{GS} = 4V$ using $\mu_n = 200\ cm^2\ V^{-1}s^{-1}$, $C_{ox} = 2.5\ fF/\mu m^2$ and $V_{Tn} = 1V$. Calculate a few points and plot $R_\square$ versus V_{GS}.
Hint: $R=R_\square\ (L/W)$





$\because V_{DS} < 0.1V < [V_{GS} - V_T \geq (1.5 - 1) = 0.5V]$

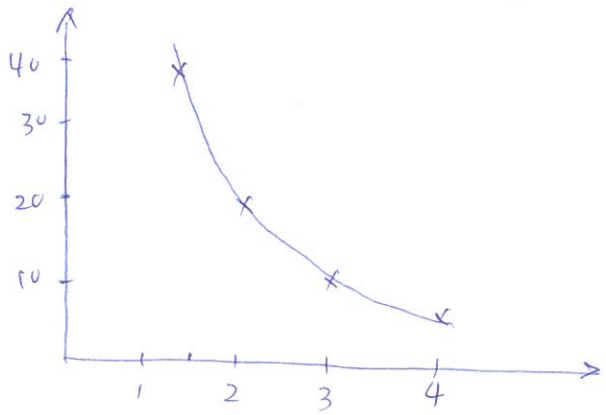
$\therefore$ Triode region

$$I_D = \mu_n \cdot C_{ox} \cdot \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$R_{DS} = \frac{V_{DS}}{I_D} = \frac{L/W}{\mu_n \cdot C_{ox} \cdot (V_{GS} - 1)} = R_\square \cdot \frac{L}{W}$$

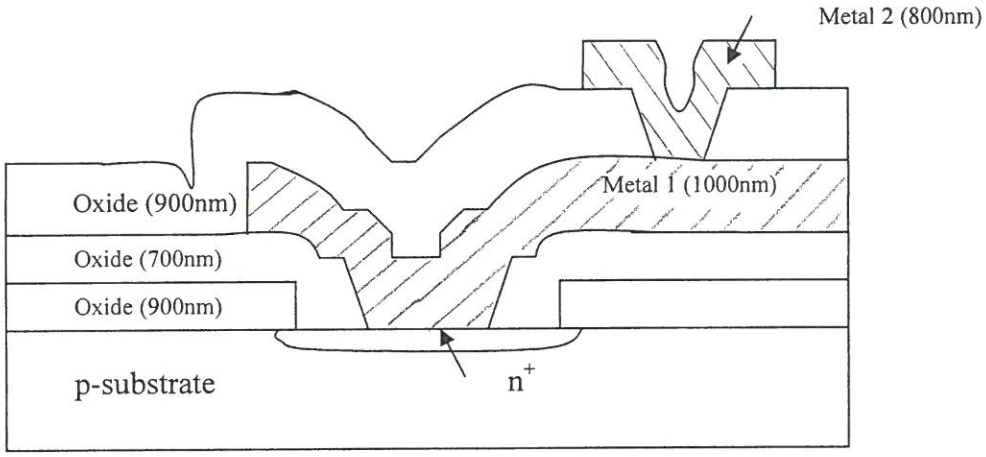
$$\therefore R_\square = \frac{1}{200\ cm^2/V\cdot s \times 2.5 \times 10^{-15}/10^{-8}\ cm^2}$$

$$= \frac{20\ k\Omega - V}{(V_{GS} - 1)}$$



6.2 (7 marks) Suggest a process sequence for the following structure starting from a p-doped wafer (ignore cleaning). Include deposition technique, material and thickness. For example, the last two steps might be:

- Sputter 0.8 μm of Al-Cu alloy
- Pattern M2 lines in PR, etch M2 and strip PR.



1. Grow 900 nm thermal oxide;
2. Pattern with n^+ mask in PR, etch SiO_2 and strip PR;
3. Ion implantation with Phorsphorus + annealing;
4. ~~Sputter~~ CVD 700 nm oxide, pattern with Metal 1 contact mask, etch oxide, strip PR;
5. Sputter Al, 1000 nm, pattern with metal 1 mask, etch Al, strip PR;
6. CVD 900 nm oxide, pattern with metal 2 contact mask, etch oxide, strip PR
7. Sputter 0.8 μm of Al-Cu alloy
   Pattern M_2 lines in PR, etch M_2 and strip PR