ECED 4260 IC Design and Fabrication

Lab 1 Individual Marking Sheet

Student Names	ID #	Lab Station #	Marks (out of 3)

Understanding VHDL (1 point):
Draw the schematic diagrams of the attached VHDL codes (i.e. Xor_2 and Xor_3).

VHDL Compilation (0.5 point):
Compile the Xor_3.vhd, and write down the following information:

Pin Assignment: _____

FPGA Device used: _Altera Cyclone ___ EP _____
Total logic elements used: _____Total pins: _____

Circuit Simulation (1 point):
Simulate the Xor_3 using **ModelSim-Altera**.

The delay of the output is about _____ns for functional simulation.

The delay of the output is about _____ns for timing simulation.

Demonstrations (0.5 point): **TA's signature**

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