ECED 4260 – IC Design and Fabrication

http://mems.ece.dal.ca/eced4260.php
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1. Logic design review
2. Hardware description language and simulation
3. Register-Transfer Level components
4. RTL level system design
5. Arithmetic circuits design
6. Digital system testing
7. Microfabrication process

Evaluation:

Assignments	6 %
Tut 1 and Lab1	6 %
Lab 2 and 3	12 %
Lab 4	15 %
Midterm	26 %
Final	35 %

Course Notes: http://mems.ece.dal.ca/eced4260/Coursenotes2016.pdf

Reference1. Peter J. Ashenden, **The Student's Guide to VHDL** (Morgan Kaufmann, 1998 or 2nd Ed.)

Reference2. Peter J. Ashenden **The Designer's Guide to VHDL** (Morgan Kaufmann, 3rd Ed.)

Reference3. M. Morris Mano, **Digital design with an introduction to the Verilog HDL, VHDL and SystemVerilog** (Pearson)

Reference4. Pong P. Chu, **RTL Hardware Design Using VHDL** (John Wiley & Sons)