DALHOUSIE UNIVERSITY

Final Project: Design of a Dice Game

ECED 4260 IC DESIGN AND FABRICATION
Department of Electrical and Computer Engineering
Fall 2023

CONTENTS

OBJECTIVES

In this lab, you will design a dice game in VHDL or Verilog and implement it on DE1-SoC boards. The project will give you experience designing with RTL descriptions, building input/output interfaces, and teach you how to approach system-level integration and optimization. At the end of this project, you should have a good understanding of the basic digital hardware development process.

DESIGN OF A DICE GAME

1 Introduction

The primary goal of this project is to familiarize ECED4260 students with the common methods and tools of digital design. In groups of two students, you will design and implement a simple dice game. You will use HDL to design this system, targeting the DE1-SoC platform. The project will give you experience designing with RTL descriptions, building input/output interfaces, and teach you how to approach system-level integration and optimization. **Functional implementation will be your primary goal**. To better expose you to real design decisions and tradeoffs, we hope you can optimize your design for cost (FPGA resource utilization) and performance (speed).

In most of the digital design projects, your first step will be to understand how to map the high-level specifications to a design which can be translated into a hardware implementation (Top entity diagrams, Architecture schematics, State transition diagrams). After that, you will design each submodule in VHDL and debug these implementations. Remember that this first step can potentially take significant time if you have not thought out your design prior to trying implementation. After you have built a working implementation, the next step will be optimizing it for speed and resource use on the target FPGA platform.

Finally, good time management and good design organization is critical to your success. Good luck!

2 Schedule

Week 10, Design ideas for Data Path and Controller.

Week 11-12, HDL coding and ModelSim testing;

Week 13, Integrate data path and controller, optimization of your implementation.

Week 14, Dec. 4 & 6, Demonstration and Project presentation.

Dec. 8th, Final Report Due.

3 Project Specification

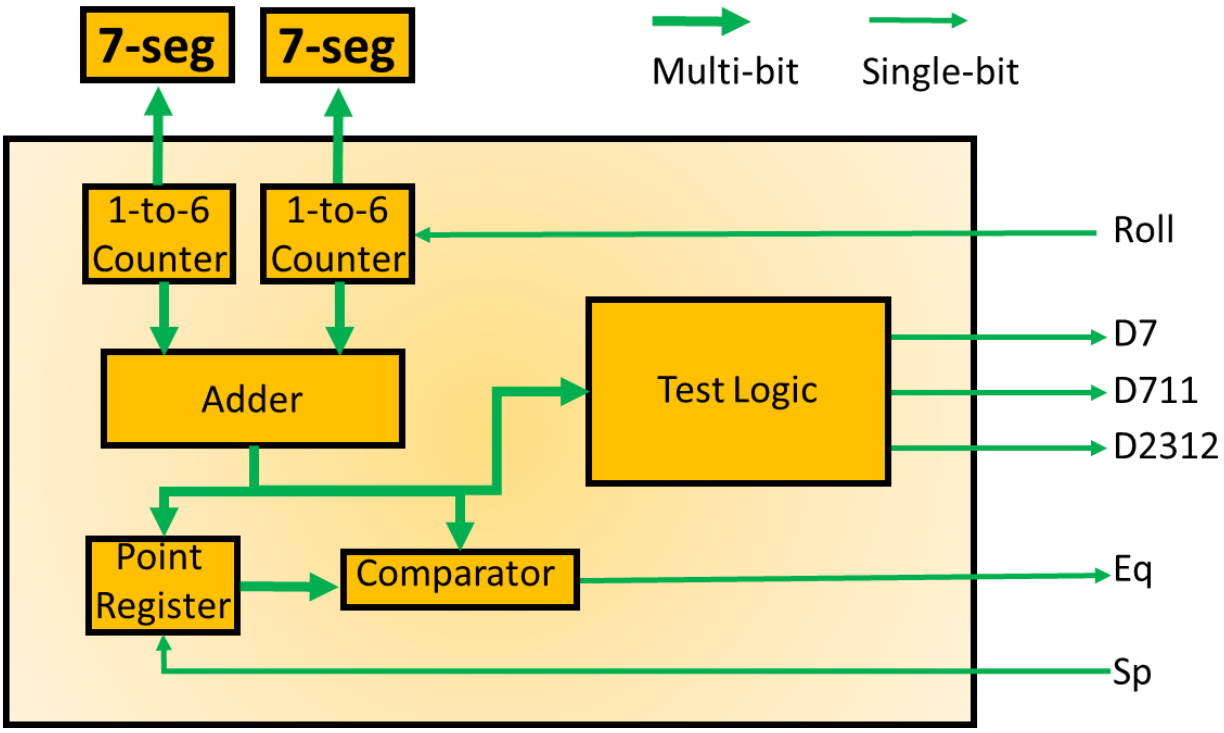
The game you will design, and implement is popularly known as **Craps**. The game involves two dices, each of which can have a value between 1 and 6. **Two pseudo-random counters are used to simulate the roll of the dice.** After the "roll" of the dice, the sum of the values in the two counters will be in the range 2 through 12. The rules of the game are as follows:

1. After the first roll of the dice, the player wins if the sum is 7 or 11. The player loses if the sum is 2, 3, or 12 (i.e. craps). Otherwise, the sum the player obtained on the first roll is referred to as a point, and he/she must roll the dice again.

2. On the second or subsequent roll of the dice, the player wins if the sum equals the point, and he/she loses if the sum is 7. Otherwise, the player must roll again until he/she finally wins or loses.

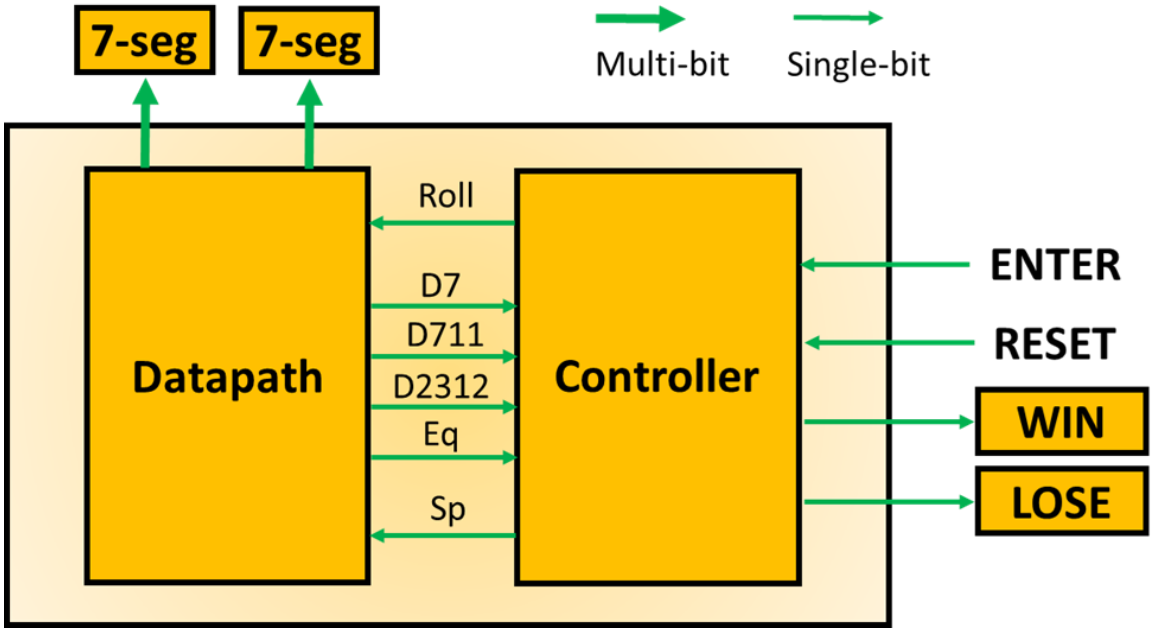
Based on the rule of the game, we can design the data path. The data path given below includes an adder, which adds the two counter outputs, a register to store the point, a comparator to compare the values stored in the point register and the output from the adder, and a test logic to determine conditions for win or lose.

Each component needs to be tested separately. All the annotated simulation waveforms should be included in the report. Then you can put all these components together to make a complete data path. Debug and test the complete data path circuit. Make sure to include the corresponding annotated simulation waveform in the report.



Next, a finite state machine can be designed as the controller of the system. Debug and simulate the FSM until it works properly. Make sure to include the FSM simulation waveform in the report.

After you finish designing and testing the data path and the controller. The final design of the system is simply an integration of the controller and the data path as shown below. Debug and simulate the final system until your design realizes the desired function. Then you are ready to demonstrate your designed system to TA. An annotated simulation waveform is also required for the final system.



The inputs to the game control come from two push buttons, "Enter (Roll Button)" and "Reset". The outputs are two 7-segment displays and two LEDs for "Win" (green) and "Lose" (red) signals. "Reset" is used to initiate a new game. When the "Roll Button" is pushed, the dice counters count at a high speed, so the values cannot be read on the 7-segment display. When the "Roll Button" is released, the values in the two counters are displayed. After rolling the dice, the sum is tested. If it is 7 or 11, the player wins; if it is 2, 3, or 12, he/she loses. Otherwise the sum is saved in the point register, and the player rolls again. If the new sum equals the point, the player wins; if it is 7, he/she loses. Otherwise, the player rolls again. If the "Win" light or the "Lose" light is not on, the player must push the "Roll Button" again to keep playing. After winning or losing, he/she must push "Reset" to begin a new game. The push buttons on the FPGA board are properly debounced.

Other signals are defined as follows:

D7 = 1 if the sum of the dice is 7

D711 = 1 if the sum of the dice is 7 or 11

D2312 = 1 if the sum of the dice is 2, 3, or 12

Eq = 1 if the sum of the dice equals the number stored in the point register

Roll = 1 enables the dice counters

Sp = 1 causes the sum to be stored in the point register

Win = 1 turns on the win light

Lose = 1 turns on the lose light

DEMONSTRATION

You will need to demonstrate your designed system on a FPGA board to the TA/instructor in the lab.

LAB REPORT INSTRUCTIONS

A formal report is required for this project. A guideline on how to write your report will be posted on the course website.

GRADING[1,2]

Report (50%)		Presentation (50%)
Demonstration	(30%)	
Abstraction & Introduction	(10%)	
Design process, simulation and testing method	(35%)	---
Discussion & Conclusion	(15%)	
Presentation (clarity, neatness, format etc.)	(10%)	

- Lab report and project presentation each account for 50% of the total score of the final project.

Good luck!