Report Guidelines

Report Contents

The following is an outline of what is expected to be included in the report for the final project.

- **Title Page**
- **Table of contents**
- **Abstract** - a concise summary of the contents of the project. The abstract should appear by itself on the first page after the table of contents.
- **Introduction** - a brief description, in your own words, of the lab problem.
- **Design Section –** describes the design of your solution to the lab problem using your own words. It is highly recommended that you use schematics, diagrams, flow charts, tables and VHDL files to help you explain the designing process. This section should be very detailed and descriptive. All diagrams, schematics, flow charts, tables should be neatly drawn. If a diagram is hand drawn, it must be drawn using a straight edge, preferably on engineering graph papers.
- **Simulation & Testing** - consists of two parts. You must describe, in the body of your report, the strategy behind your testing sequences (ie. Why are you using this test sequence, and why is this a good test?). Describe your inputs and expected outputs. The second part of testing is explaining the results. Are the results of your simulation, as displayed on the waveforms, showing the desired function? All of this should be explained in detail in the body of the report, with references made to the annotated waveforms. All waveforms should be clearly annotated, and testing sequences should be pointed out.
- **Discussion & Conclusion** - summarizes the results of your work. Discuss the questions you have encountered in the designing process and how you solved the problem eventually. Does your design solve the given lab problem? What are the future works? What could be done to make your design better? Did you do any optimization work for your design?
- **Appendix** - ALL VHDL files and other reference items. All appendix items should be clearly labelled.

Report Format and Presentation

- Lab reports must be typed. Handwritten reports will not be accepted. Handwritten additions to the appendix materials are acceptable, provided the writing is clear and legible.
- Use page numbering, a table of contents is useless without page numbers.
- The language and style of the report should be formal.
- Spend time developing the flow of your report. Its readability will have a strong influence on how well it is received (translation: easier to read, easier to mark, higher mark).
- Check your spelling and grammar. The spell checker exists for a purpose, use it.
- All appendix items should be clearly labelled, and, in the case of diagrams, neatly drawn. If a diagram is hand drawn, it must be drawn using a straight edge, preferably on Engineering Graph Papers.

- The names and ID numbers of your group members must be included in each VHDL file (ie typed into the file header) included with your report.
- Each figure/diagram should have a caption. Waveform annotations should be useful but don't go overboard and make the waveforms hard to understand due to the barrage of comments on the printout.

Marking and Major Deductions

The reports will be marked following the marking rubrics posted by TA on Brightspace.

Major deductions are as follows:

- A report without all required VHDL files will be deducted 30% of the report mark.
- Late reports are deducted 20% of the report mark per day, up to a maximum of 3 days. Reports more than 3 days late will not be accepted.
- Failing to include your names and ID#'s in all of your VHDL files and a summary of your contribution to the project will result in a deduction of 10% of the report mark.
- No annotations on your waveforms will result in a mark only for handing in the report.