DALHOUSIE UNIVERSITY
FACULTY OF ENGINEERING

Department of Electrical and Computer Engineering

ECED 4260/Credit Hours: 3/IC Design and Fabrication

Fall 2024/2025
Lectures (Mon. & Wed. 13:05-14:25 at D501)
Tutorial / Lab (Fri. 14:05-15:55)
Delivery Method: face-to-face
Course Website: mems.ece.dal.ca/eced4260.php

Instructor: Yuan Ma
Office: Sexton Campus C314
Office Phone: (902) 494 6129
Office Hours: Tue. 1-3 pm at C314
Email: Yuan.Ma@Dal.Ca

Individual meetings can be scheduled by appointment via email. In any email regarding this course, please include "ECED 4260" in the subject, and I will make every attempt to reply to your email within 24 hours except the weekends.

TA & Marker	Justin Greige
Email:	Js488811@dal.ca

Course Description

The theory of MOS transistors is reviewed at the beginning of the course and their fabrication technologies are presented with an emphasis on CMOS circuit fabrication. Design and modelling of RTL (Register Transfer Level) digital system are then introduced using hardware description languages VHDL and Verilog. Subsystem design of arithmetic circuits, ROM, RAM and FSMs will be examined and implemented with Field Programmable Gate Arrays (FPGA) training board DE1-SoC. Performance analysis, optimization, faults, and testability will also be discussed. Extensive use of CAD tools will give the student hands-on experience with systems typical of those used in industry.

Course Pre-requisites, Co-requisites and/or other Restrictions

ECED 2200 Digital Circuits, and ECED 3201 Introduction to Electronics

Course Rationale and/or Other Restrictions and Requirements

This course covers high level digital system design of the Electrical and Computer Engineering program. The modernized labs with Field-Programmable Gate Array (FPGA) boards prepare students for innovative Register-Transfer-Level (RTL) solutions from their design through their implementation. The attendance to the tutorial and lab sessions is mandatory.

Short-term Missed Work and Absence Reporting

Any absence resulting in missed academic work must be reported using the Engineering Student Absence Reporting online system. This applies to both *Student Declaration of Absence* and *Request for Accommodation*. Visit forms.engineering.dal.ca for details and to submit a request.

The following policies will apply to assessments missed due to self-declared absences:

- Any missed assignments may be submitted late without penalty up to the time when solutions are posted. After that time, the final mark in the course will be substituted for the assignment mark.
- Missed lab must be completed as soon as possible on student's own time.

Supplemental Exam

If you miss the midterm exam for an approved absence, a supplemental midterm will be provided.

Course Learning Outcomes

Upon completion of this course, you should be able to:

- Understand and apply classical sequential logic design in general digital circuits.
- Demonstrate use of hardware description language using computer aided tool such as Intel Quartus Prime.
- Design and test RTL (Register Transfer level) digital system.
- Apply the solution of fast addition and multiplication to binary numbers.
- Demonstrate independent learning skills.

Recommended Text(s)

Peter J. Ashenden, The Student's Guide to VHDL, and The Designer's Guide to VHDL
M. Morris Mano, Digital Design with an Introduction to the Verilog HDL, VHDL and SystemVerilog
Pong P. Chu, RTL Hardware Design Using VHDL

Experiment Kit (provided for in-person labs): Intel DE1-SoC board.

Course Schedule

An important part of the course is to develop RTL design skills through lectures and labs. Three tutorials, three labs and one project are designed for this purpose. Please refer to the course website for tutorial/lab procedures.

	Focus Topic	**Tutorial/Lab Activities**	**Assessments**
1	Introduction	-------	------
2	HDL and FPGA introduction	Tutorial A. Quartus Prime	Tutorial A
3	Synthesizable VHDL constructs	Tutorial B. ModelSim simulator	Assignment 1/Tutorial B
4	Testbench and timing analysis	Tutorial C. Testbench	Tutorial C
5	Micro-fabrication	Lab 1. Arithmetic circuit HDL	Assignment 2/Lab1
6	RTL design	Lab 2. Multiplier and FSM	Lab2
7	Arithmetic circuits	Midterm	Assignment 3
8	Finite state machine	Lab 3. RTL Design	Lab 3

	Focus Topic	Tutorial/Lab Activities	Assessments
9	Fault model & arithmetic circuit	Project Datapath and Controller	Assignment 4
10	RAM and ROM	Project Cont'd	Project proposal
11	-------	-------	-------
12	Digital system testing	Project Cont'd	-------
13	FPGA implementation	Project presentations	Project report
14	Review	Project presentations	

Course Assessments

Components of your grade include assignment, tutorial/lab, midterm, and design project.

Assignments (20%): Four assignments will be set and evaluated as part of the learning process. Unless specifically indicated, every assignment is to be completed independently.

Tutorial and Labs (20%): Please refer to the course website for the schedule and requirement of tutorial/lab submissions. Students are recommended to download the Intel Quartus Prime software onto their own computers. The instruction for downloading the software and the user guides of the FPGA programming boards used in the lab can be found on the course website.

Midterm (30%): The midterm will be scheduled in Week 7 to evaluate the learning outcomes of the courses.

Project (30%): Students will work individually or as a team of two students on the design of an RTL system. Presentations on the design, simulation and testing of the system are required near the end of the term. Additional information on this project will be provided in class as well as posted in Brightspace.

University Statements

https://dalu.sharepoint.com/sites/acad/eng/SitePages/Course-Syllabus-Appendix.aspx

Associate Deans Office – Undergraduate Studies

Associate Dean: Dr. Darrel Doman darrel.doman@dal.ca
Undergraduate Office Coordinator: Jason Lecoure Jason.lecoure@dal.ca
Student Success Coordinator: Karyn Hemsworth Karyn.hemsworth@dal.ca
General Inquires: engineering@dal.ca or (902) 494-2963

Dalhousie Engineering Student Oath

I, as one who is preparing to enter the profession of engineering, promise to conduct myself in an honorable and ethical manner, and, as such, I will not cheat, plagiarize or be involved in any other academically dishonest activities. I shall uphold the values of truth, honesty and trustworthiness. I shall study diligently so that I will be able to safeguard human life, to protect the welfare of society and the environment, and to uphold the reputation of the profession. In all this I shall be concerned for the well-being of others, and not just myself.