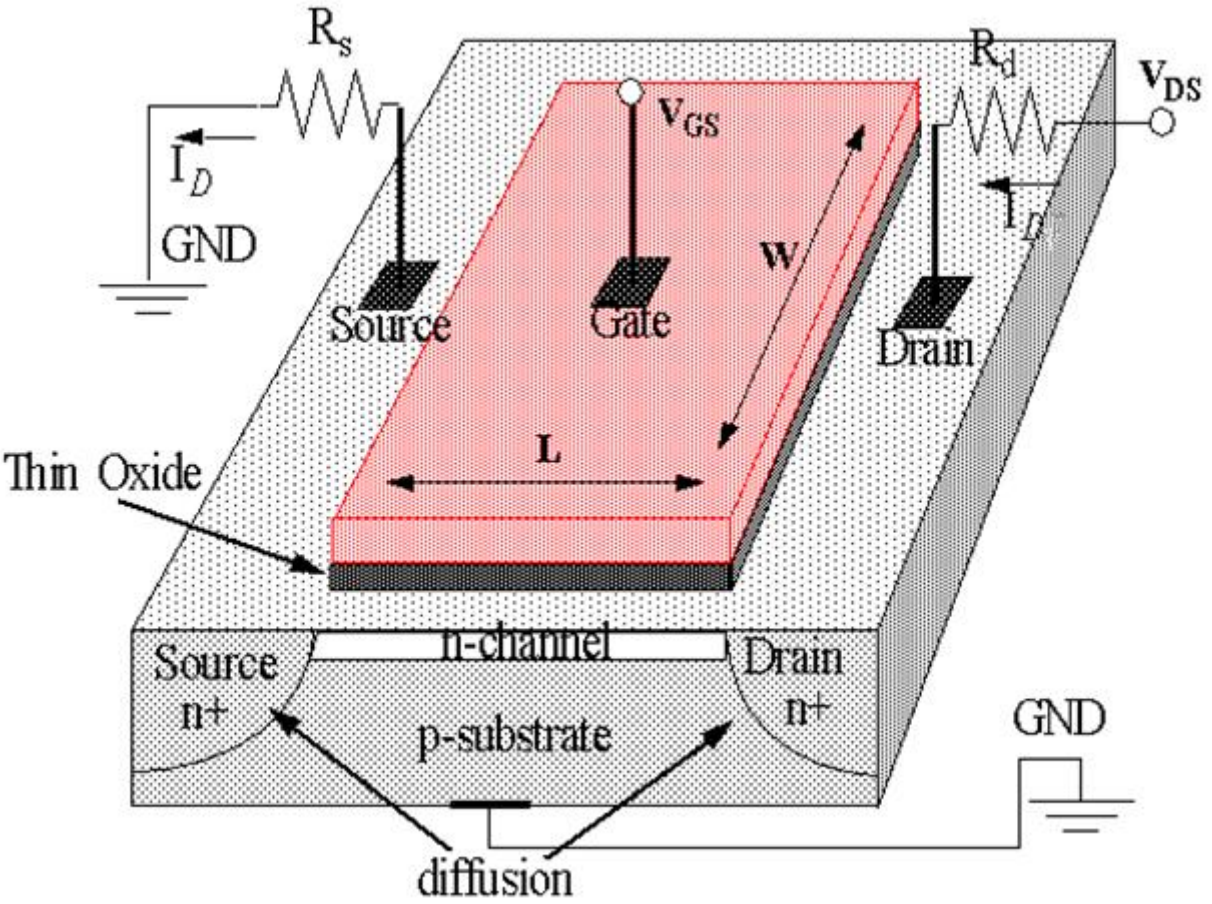
Unit 1. MOS Transistor and Micro-Fabrication

1. Basic Transistor Characteristics

1.1 MOSFET Behavior



M **metal (gate)**
O **oxide**
S **semiconductor**

n^- **$<10^{15}$ atoms /cm^3**
n^+ **$>10^{18}$ atoms /cm^3**
Si **$5x10^{22}$ atoms /cm^3**

p dopant	boron	(3 valence electrons)
n dopant	phosphorous or arsenic	(5 valence electrons)

For $0 < V_{DS} < (V_{GS} - V_T)$, the transistor operate in the triode region, also called the linear region.

$$I_D = \mu_n c_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^{\,2}\right]$$

$k_n' = \mu_n C_{ox}$ is called *process transconductance parameter*

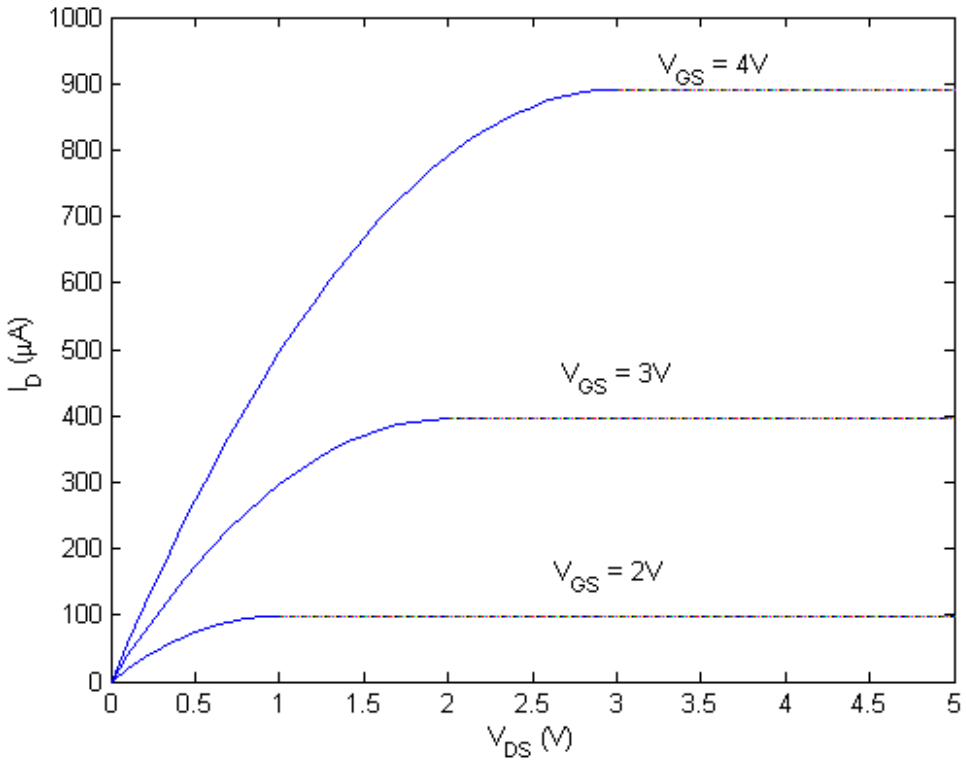
$$c_{ox} = \frac{\varepsilon_{ox}}{t_{ox}};\ \varepsilon_{ox}\ permittivity;\ t_{ox}\ thickness$$

μ_n is the average mobility of electrons in the channel.

C_{ox}: gate oxide capacitance per unit area

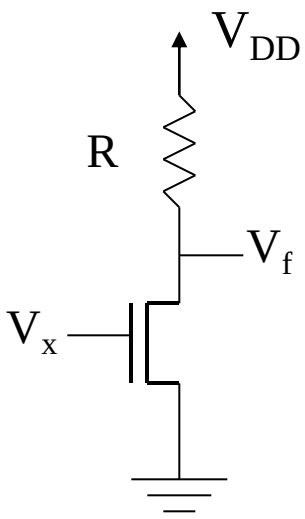
When $V_{DS} = V_{GS} - V_T$, the transistor is in the saturation region.

$$I_D = \mu_n c_{ox} \frac{W}{2L}(V_{GS} - V_T)^2$$



The current-voltage relationship in the NMOS transistor

1.2 Voltage Levels in Logic Gates



$$V_f = V_{DD} \frac{R_{DS}}{R_{DS} + R};$$

$$R_{DS} = V_{DS} / I_D = 1 / \left[k_n' \frac{W}{L} (V_{GS} - V_T) \right]$$

For

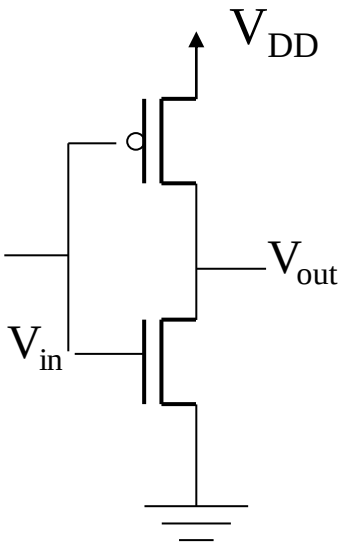
$$k_n' = 60\mu A / V^2, W / L = 2.0\mu m / 0.5\mu m, V_{GS} = 5V, and$$

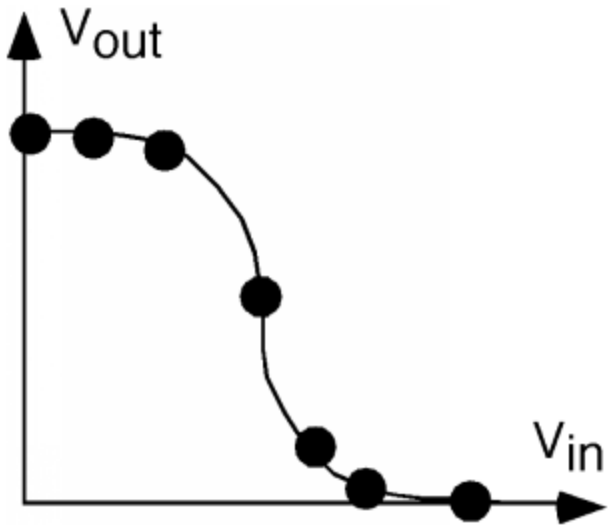
$$V_T = 1V, R_{DS} \approx 1k\Omega$$

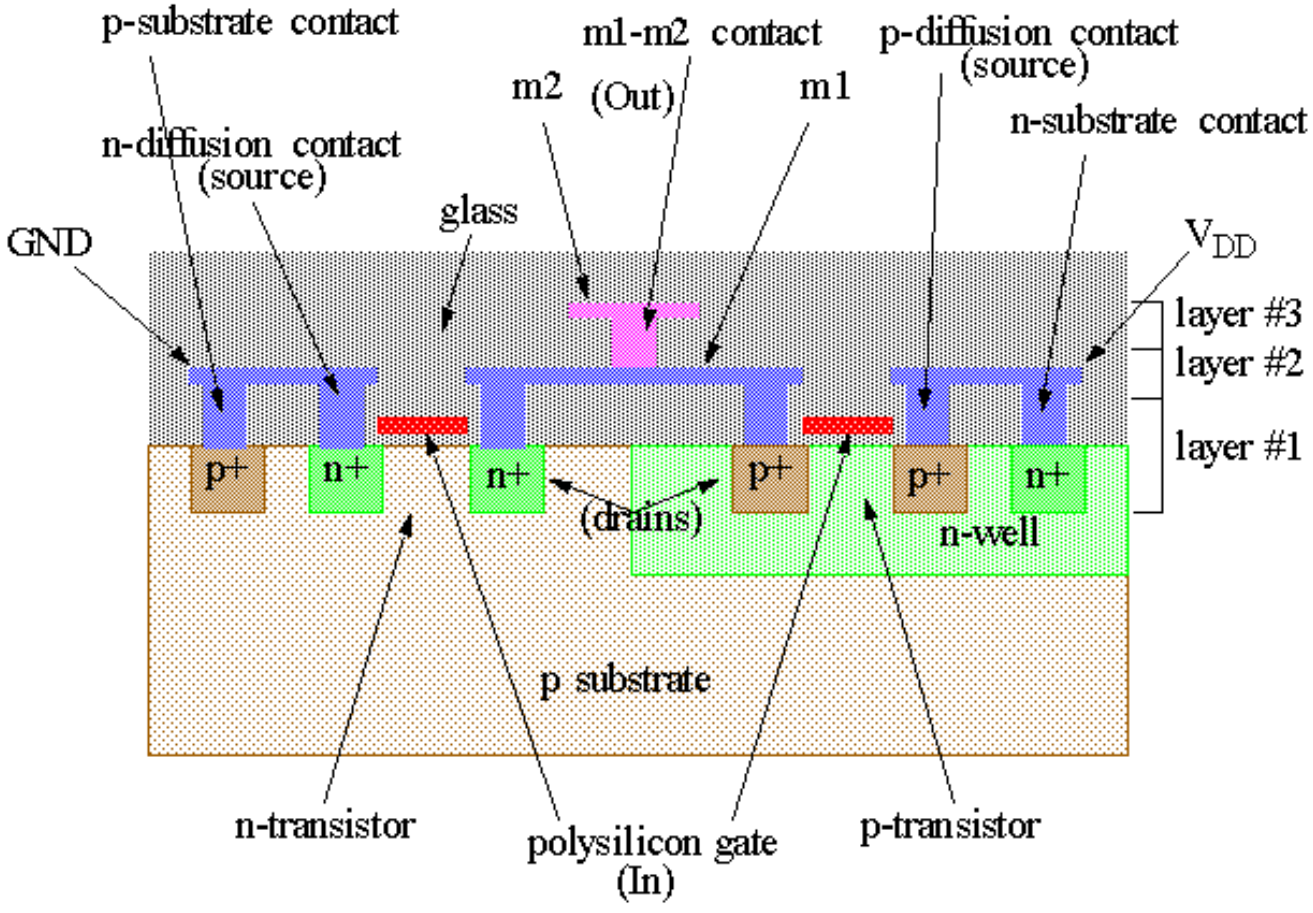
For

$$R = 25k\Omega, V_f \approx 0.2V$$

1.3 CMOS Inverter





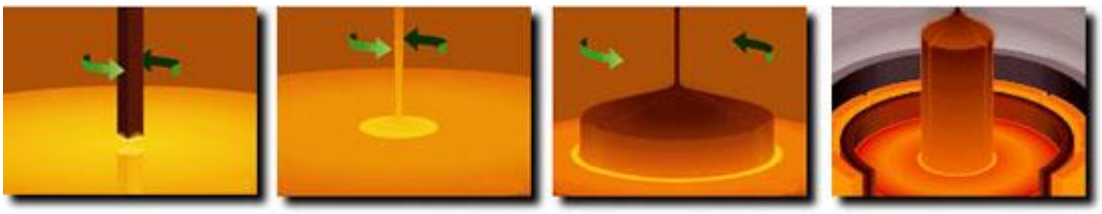


Cross-section of a CMOS inverter

2. Fabrication Technology

2.1 Wafer Manufacturing

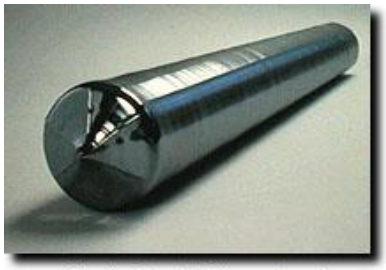
I. Crystal Pulling – Czochralski (CZ) method



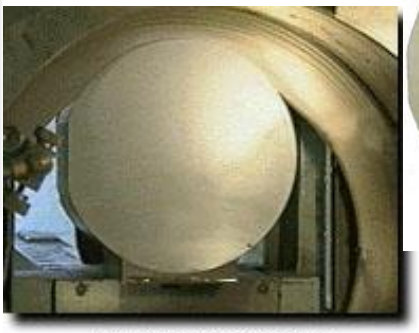
- Doped polycrystalline silicon melted at 1400 °
- Inert gas atmosphere of high-purity argon
- Single crystal silicon “seed” is placed into the melt and slowly rotated as it is “pulled out”.
- Single crystalline ingot diameter is determined by a combination of temperature and extraction speed.
- The ingots are characterized by the orientation of their silicon crystals. One or two “flats” are ground into the diameter of the ingot.

II. Wafer slicing

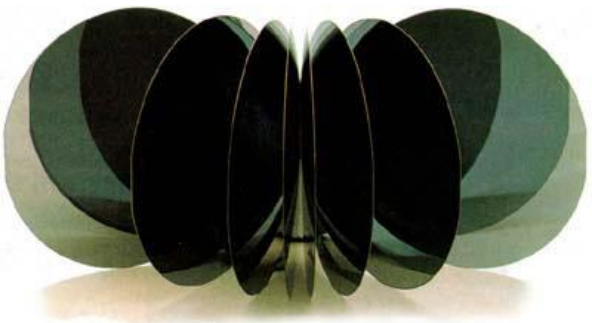
- After characterization, the ingot is sliced into individual wafers with precision “ID Saw”.



Single Crystal Silicon Ingot

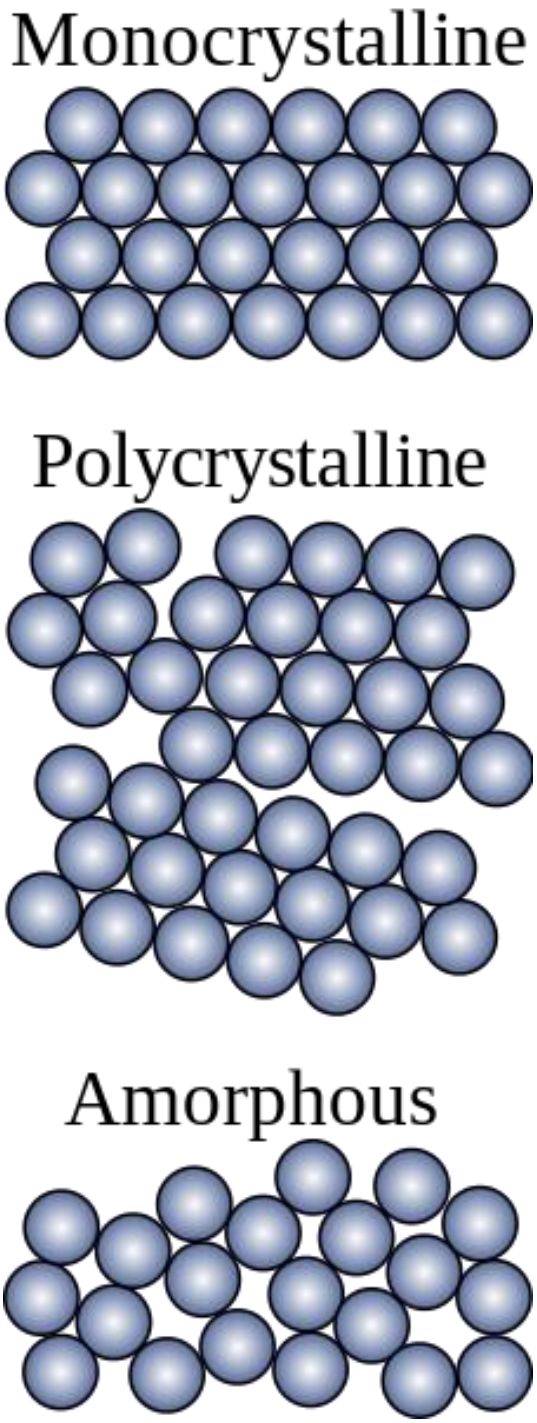


ID Wafer Slicing Saw



Ingots sliced into 450µm thick wafers, using a diamond/ID/Wire saw

https://www.tel.com/museum/magazine/material/150430_report04_03/02.html



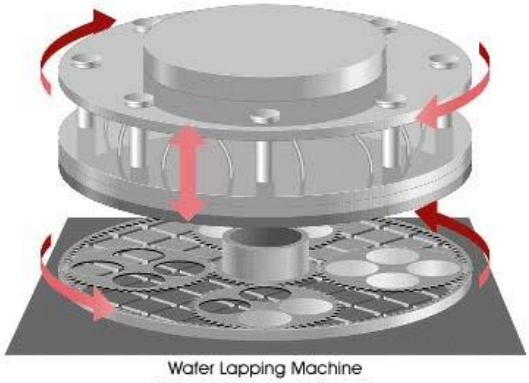
- **Monocrystalline silicon**: the crystal structure is homogeneous throughout the material; the orientation, lattice parameter, and electronic properties are constant throughout the material
- **polycrystalline silicon (poly-Si)** is composed of many smaller silicon grains of varied crystallographic orientation
- **Amorphous silicon (a-Si)** has no long-range periodic order.

https://en.wikipedia.org/wiki/Crystalline_silicon

III. Wafer lapping, etching

• The sliced wafers are mechanically lapped using a counter-rotating lapping machine and an aluminum oxide slurry to **flatten the wafer surface**, makes them parallel and reduces mechanical defects.

• Wafers are then etched in a solution of nitride acid / acetic acid to **remove microscopic cracks or surface damage** followed by a series of high-purity RO/DI water baths.



Wafer Lapping Machine
(Mitsubishi Materials Silicon)

Wafer Polishing
(Strasbaugh Corporation)

IV. Wafer polishing and Cleaning

• Next, the wafers are polished in a series of combination **chemical and mechanical polishing** processes called CMP.

• The polishing process usually involves two or three polishing steps with progressively finer slurry and intermediate cleanings using RO/DI water.

• An SC1 solution (ammonia, hydrogen peroxide and RO/DI water) is used for final cleaning to remove organic impurities and particles. Next, natural oxide and metal impurities are removed with HF and finally SC2 solution causes super clean new natural oxides to grow up on the surface.

V. Wafer epitaxial processing

• A process called epitaxy (EPI) is used to grow a layer of single crystal silicon from vapor onto a single crystal silicon substrate at high temperatures.

• The growth of a single crystalline silicon layer from the vapor phase is called vapor-phase epitaxy (VPE).

$SiCl_4 + 2\,H_2 \leftrightarrow Si + 4HCl$

(silicontetrachloride)

The reaction is reversible i.e. if HCl is added Si is etched from the surface of the wafer. Another non-reversible reaction that produces Si is,

$SiH_4 \rightarrow Si + 2H_2$

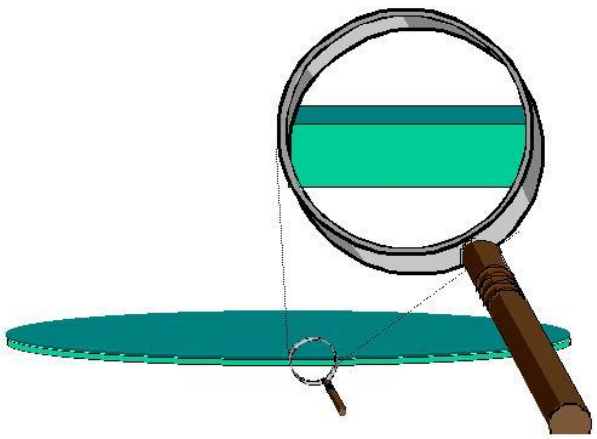
(silane)

Epitaxial Reactor
(Mitsubishi Materials Silicon)

• The purpose of EPI growth is to create a layer with different, usually lower, concentration of electrically active dopant on the substrate. For example, an n-type layer on a p-type wafer.

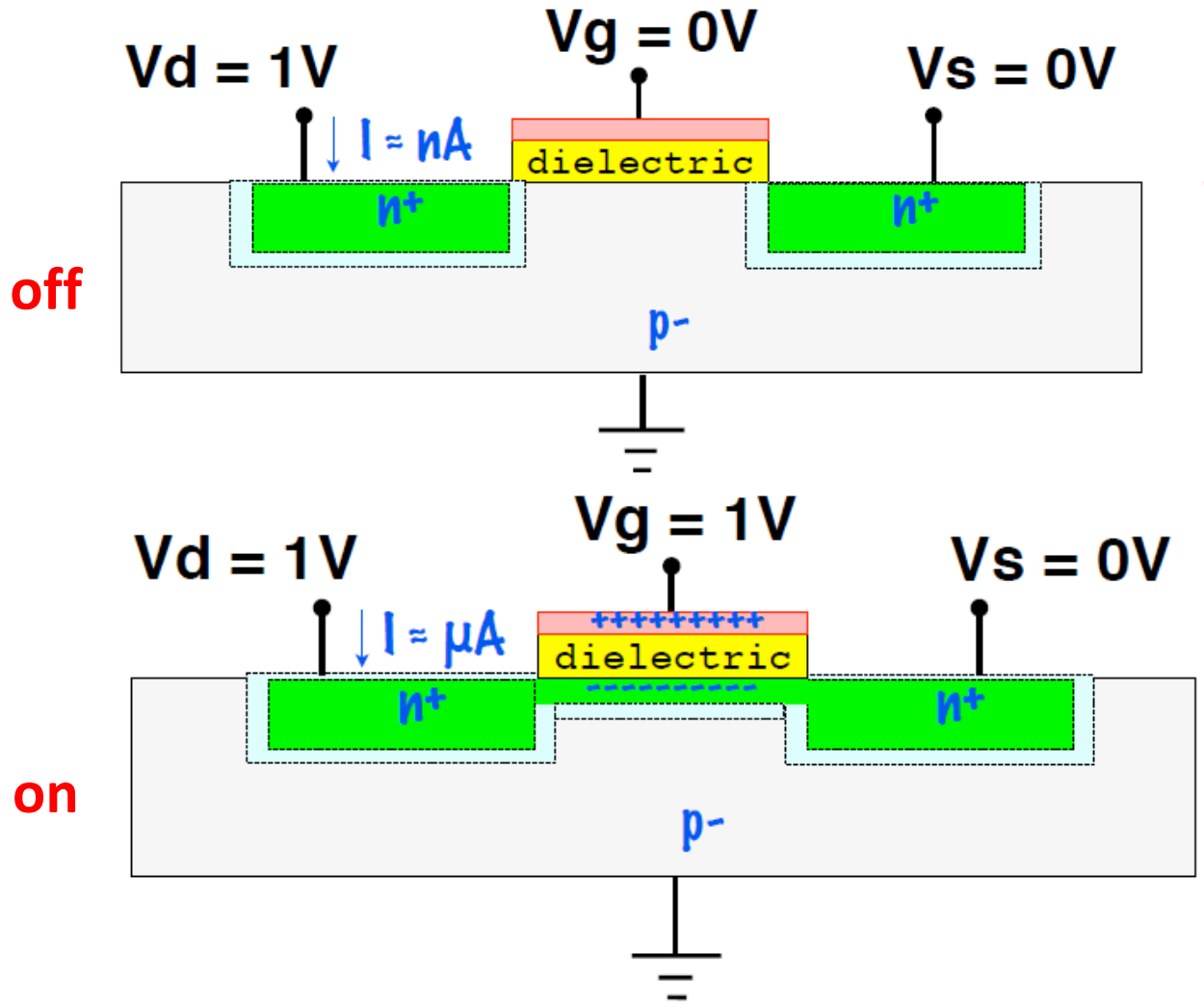
• Approx. 3% of wafer thickness.

• Contamination free for the subsequent construction of tranisistors.

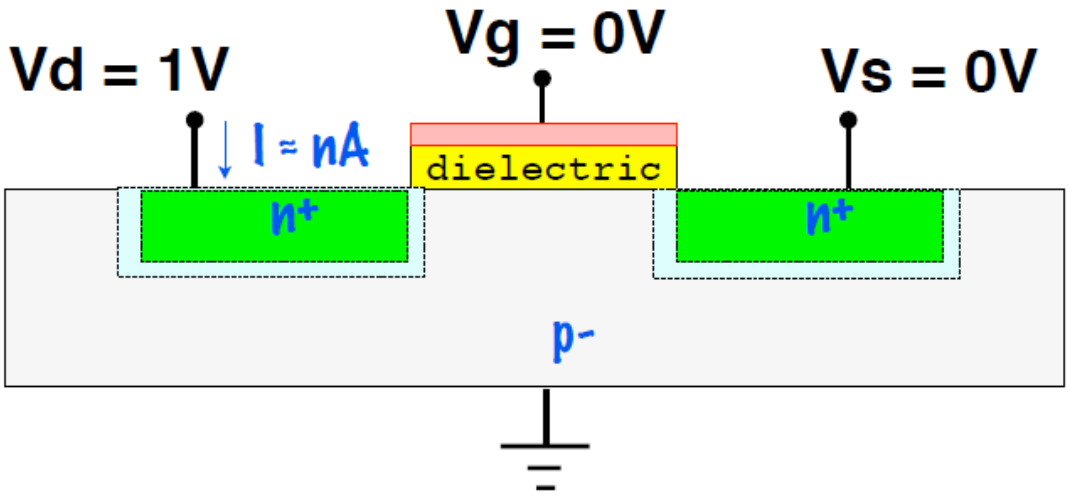


2.2 The Semiconductor Manufacturing Process

Example: N-channel MOS transistor



- Polysilicon gate, dielectric, and substrate form a capacitor
- Vg = 1V, small region near the surface turns from p-type to n-type.

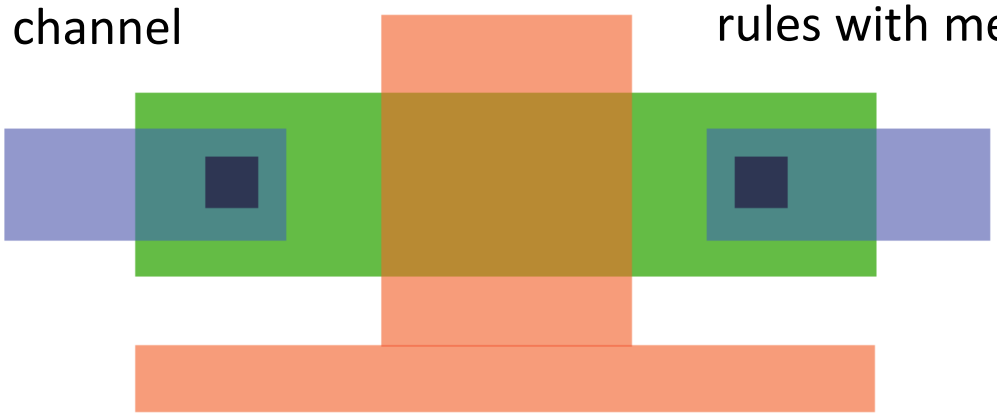


Mask top-down view:

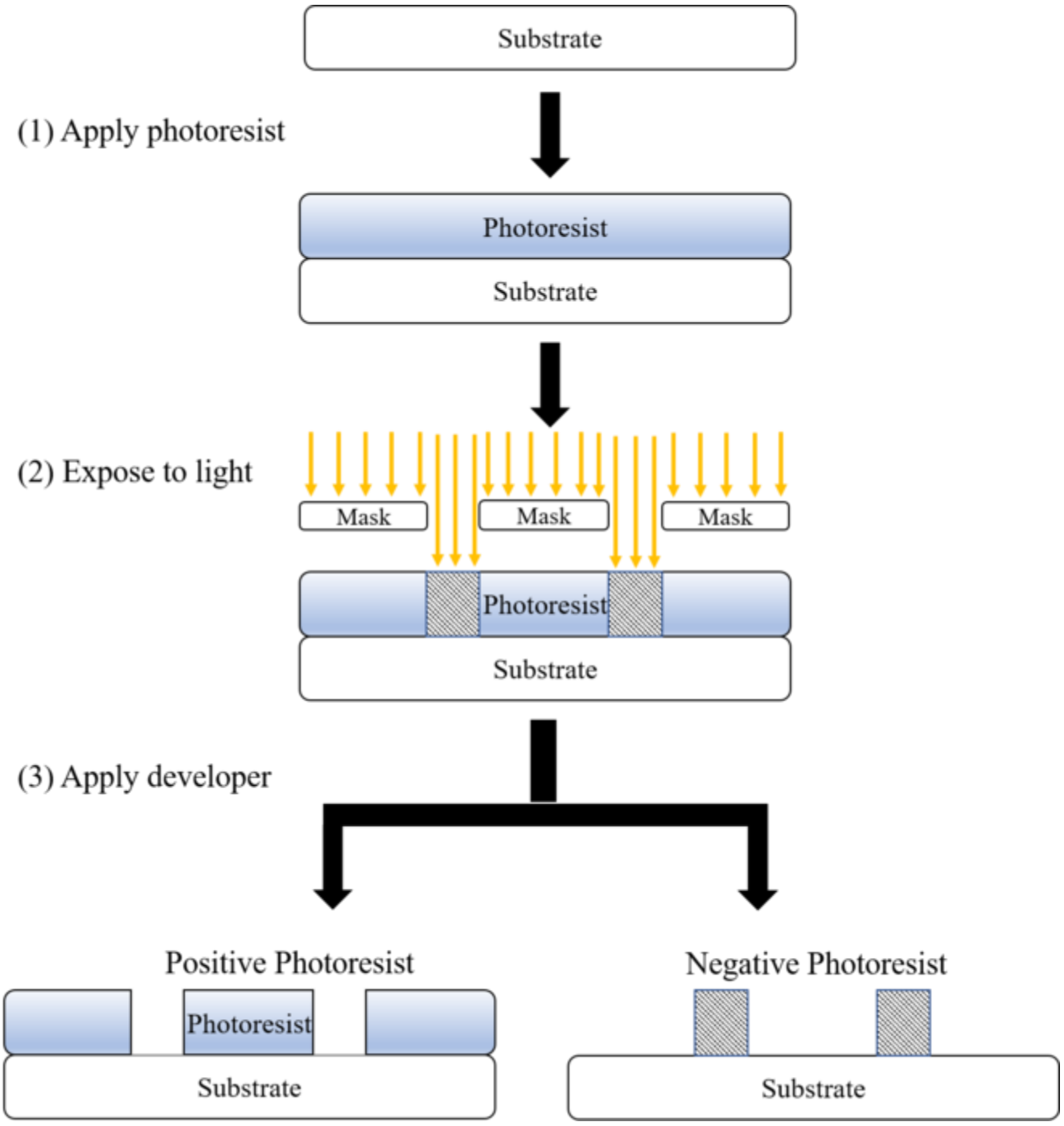
Poly overhang. So that if masks are misaligned, we still get channel

Minimum gate length. So that the source and drain depletion regions do not meet

Metal rules: Contact separation from channel, one fixed contact size, overlap rules with metal, etc



poly (gate) n+ diffusion contact metal

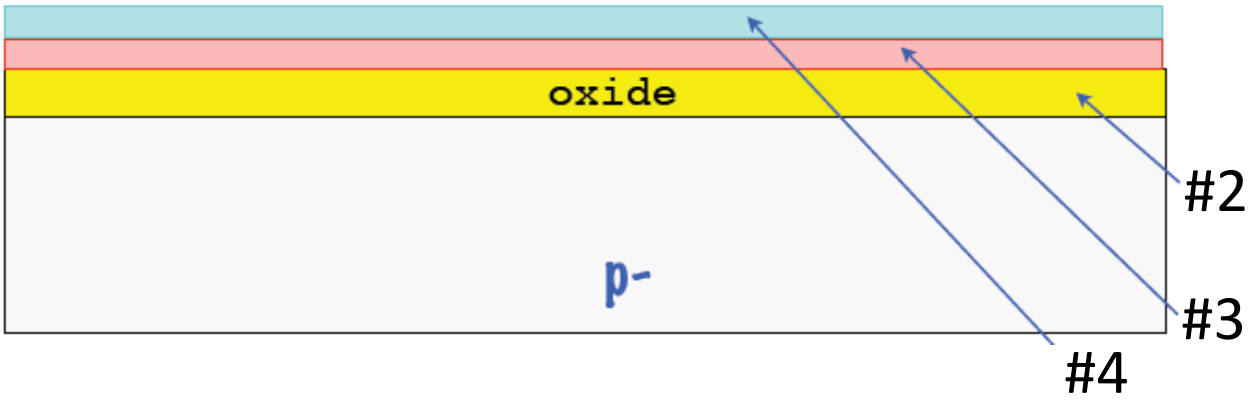


Positive – exposure to light breaks down complex molecular structure, making it easy to be dissolved.

Negative – exposure to light causes molecular structure to become more complex and more difficult to be dissolved.

https://en.wikipedia.org/wiki/Photoresist

2.2.1 Thin Film Deposition (part A)



Start with an un-doped wafer:

1. **Dope wafer p-type**
2. **Grow gate oxide**
3. **Deposit polysilicon**
4. **Spin on photoresist**

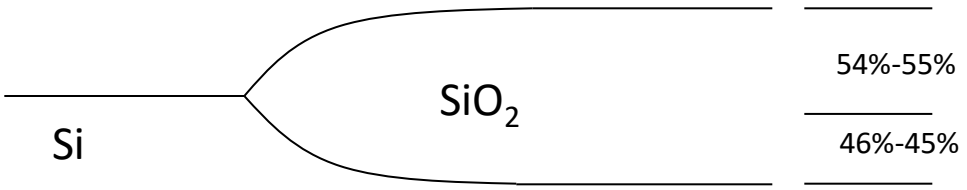
I. Silicon oxidation

SiO_2 grows thermally when silicon is in the presence of oxygen. Oxygen comes from oxygen gas or water vapor. A temperature of 900 to 1200 ^oC is required.

The chemical reactions that occur are

- $Si + O_2 \rightarrow SiO_2$
- $Si + 2H_2O \rightarrow SiO_2 + 2H_2$

- The surface of the silicon wafer after selective oxidation will appear as follow,



- **Both oxygen and water will diffuse through the existing SiO_2 and combine with Si to form additional SiO_2.** Water (steam) diffuses easier than oxygen, hence there is a much faster growth rate with steam.
- Oxide is used to provide insulating and passivation layers and form transistor gates. **Dry O_2 is used to form gates and thin oxide layers. Steam is used to form thick oxide layers.** Insulating oxide layers are usually about 1500 Å and gate layers are usually between 200 Å to 500 Å.

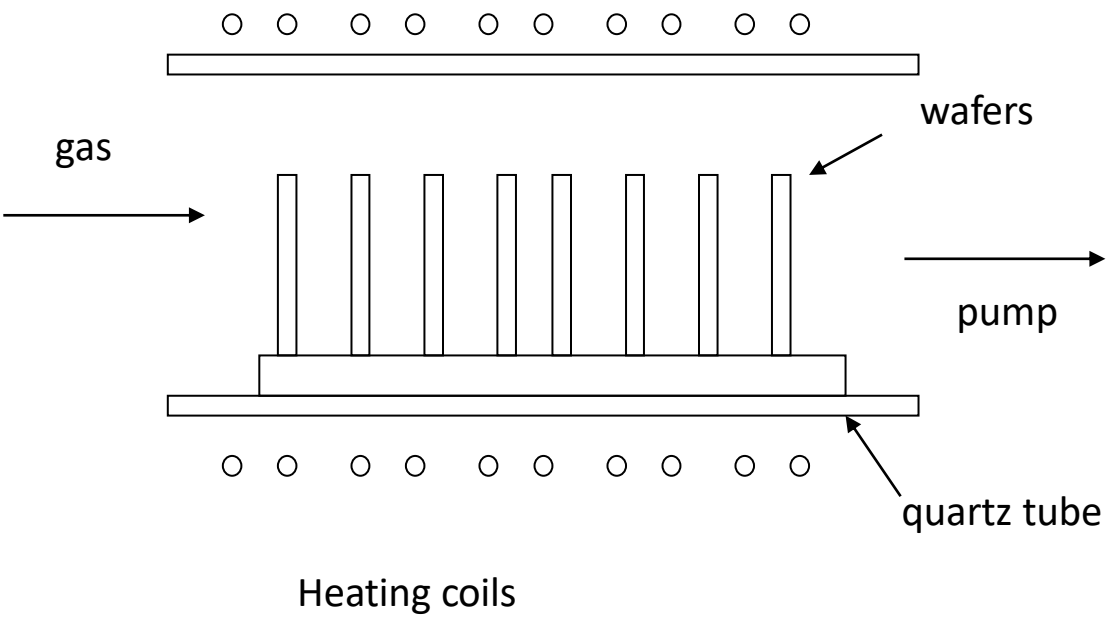
II. Chemical Vapor Deposition

• Chemical Vapor Deposition (CVD) forms thin films on the surface of the substrate by either thermal decomposition and/or reaction of gaseous compounds.

There are three basic types of reactors for CVD:

- **atmospheric chemical vapor deposition**
- **low pressure CVD (LPCVD)**
- **plasma enhanced CVD (PECVD)**

A sketch of a Low Pressure CVD process is show below,



Examples:

i) Polysilicon

$$SiH_4 \xrightarrow{600^oC} Si + 2H_2$$

Deposits 100 to 200 Å /min

- Phosphorous (phosphine), Boron (Diborane) or Arsenic gases can be addded. Polysilicon can also be doped with diffusion gases after it has been deposited.

ii) Silicon Dioxide

$$SiH_4 + O_2 \xrightarrow{300 \text{ to } 500^oC} SiO_2 + 2H_2$$

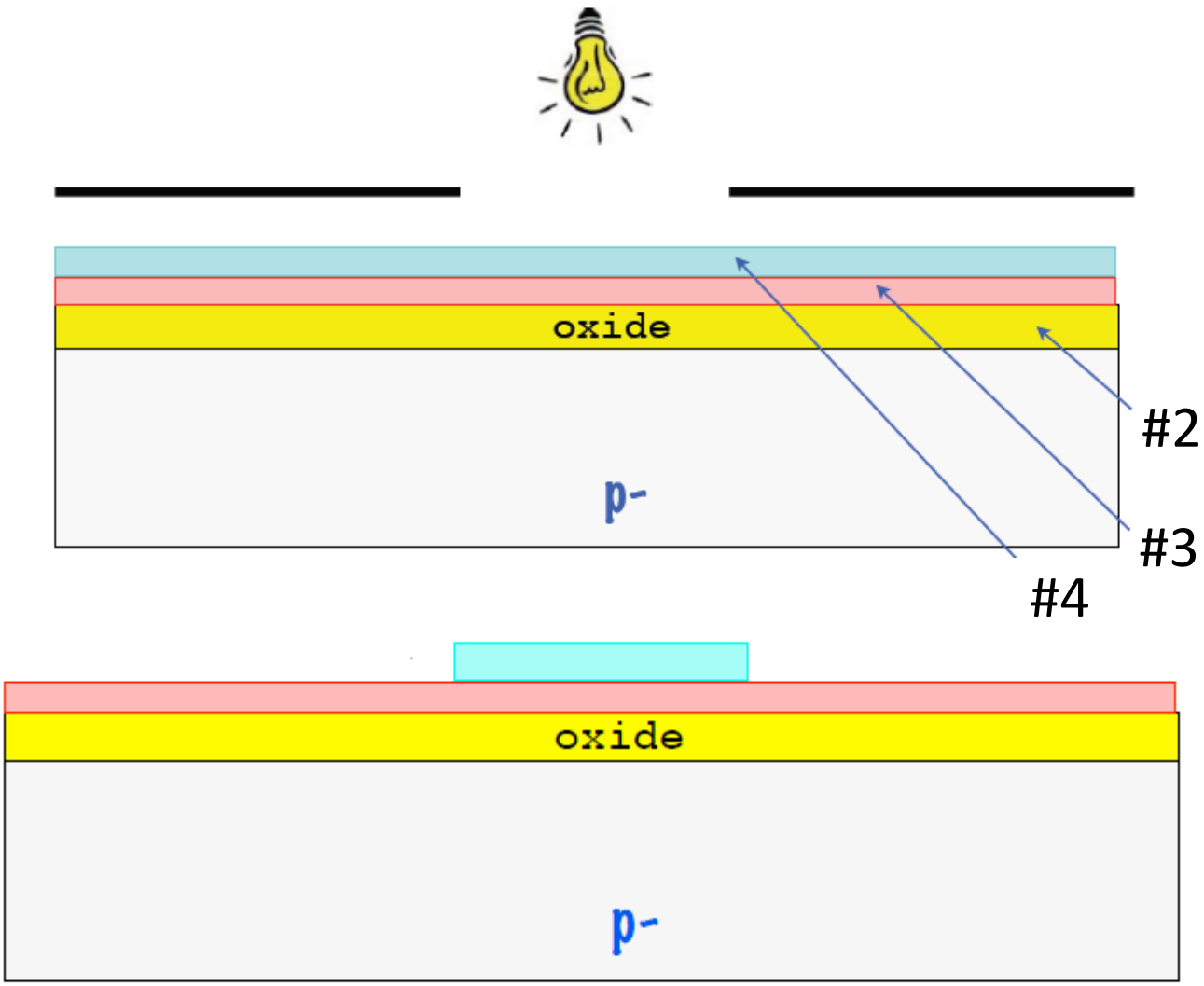
- SiO2 is used as an insulator or passivation layer. Usually phosphorous is added to give better 'flow' properties.

iii) Silicon Nitride

$$3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2$$

(silane) (ammonia) (nitride)

2.2.2 Photolithography



- Place poly mask and expose with ultraviolet (UV). UV hardens exposed resist. A wafer wash leaves only hard resist.

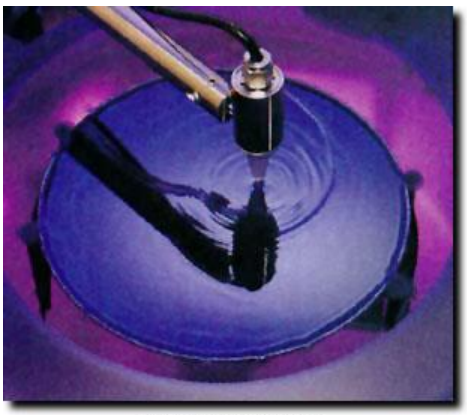
I. Photoresist coating

• Photoresist is a photo-sensitive material applied to the wafer in a liquid state in small quantities. The wafer is spun at 1000 to 5000 rpm which spreads the "puddle" into a uniform layer between 2 and 200 μm thick.

• There are two types of photoresist: **negative and positive**.
Positive – exposure to light breaks down complex molecular structure, making it easy to be dissolved.
Negative – exposure to light causes molecular structure to become more complex and more difficult to be dissolved.

The steps involved in each photolithography step are as follows;

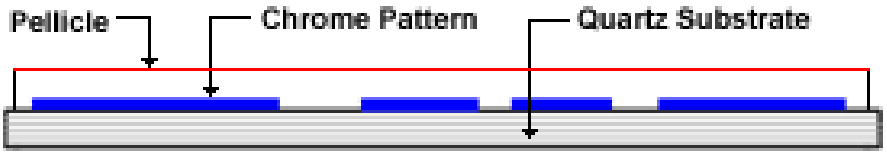
- **clean wafers**
- **deposit barrier layer SiO_2, Si_3N_4, Metal**
- **coat with photoresist**
- **soft bake**
- **align masks**
- **expose pattern**
- **develop photoresist**
- **hard bake**
- **etch windows in photoresist**
- **remove photoresist**



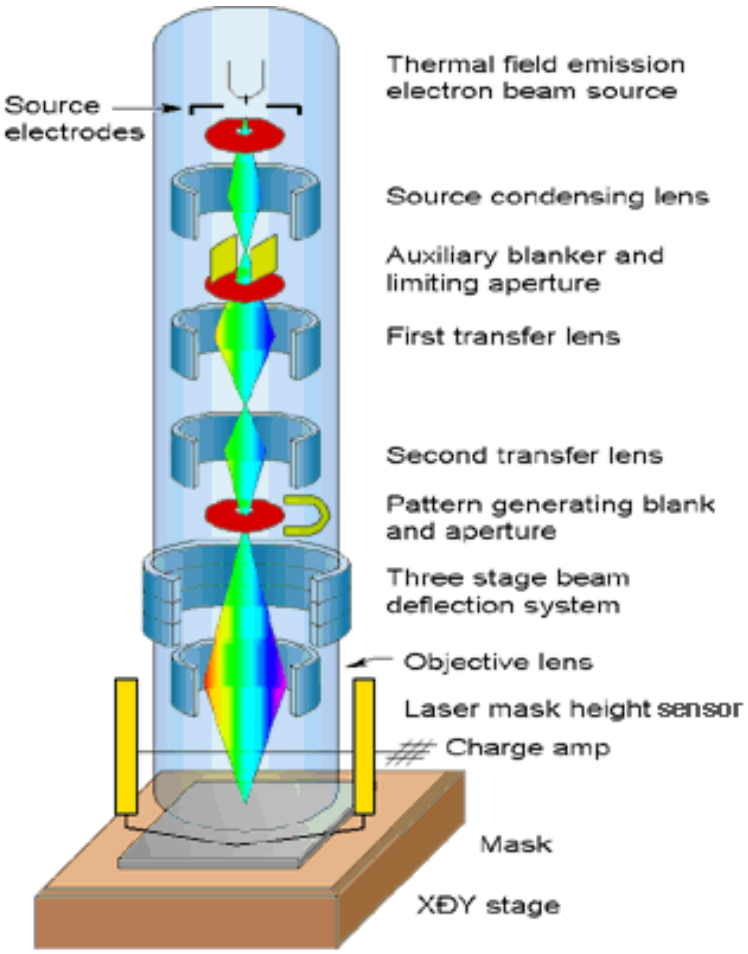
Photoresist Application
(Ontrak)

II. Pattern Preparation

• IC designers design the **pattern (mask)** for each layer using CAD software. The pattern is then transferred to an optically clear quartz substrate **(reticle)** with a chrome pattern using a **laser pattern generator** or an **e-beam**.



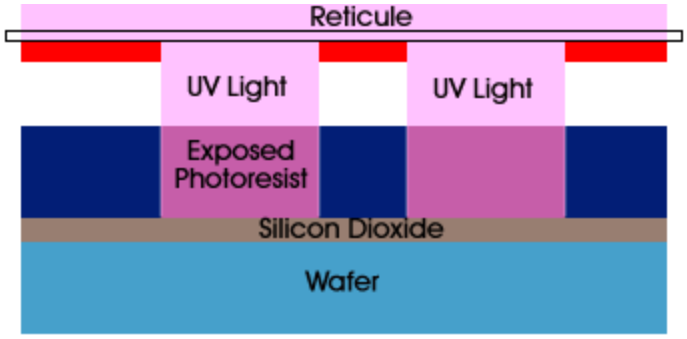
Reticle



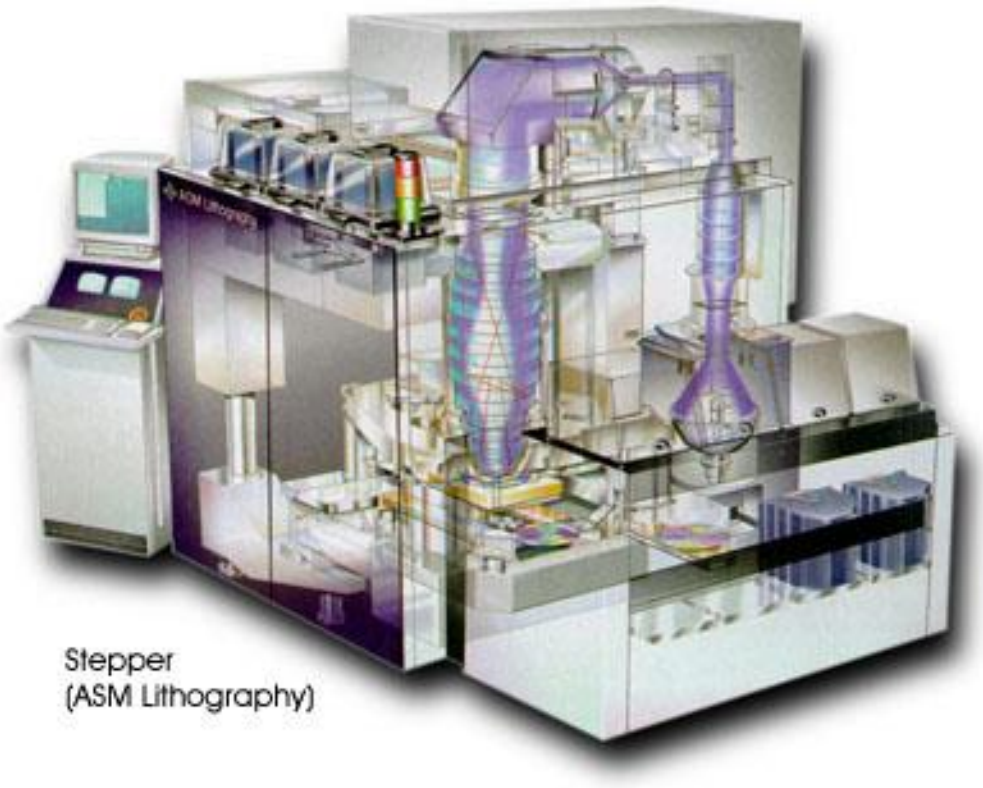
E-Beam Pattern Generator
(Etec Corporation)

III. Device layer pattern transfer

• Applying and exposing photoresist to create a device layer on an actual wafer is similar to the process used to create reticles. For actual production, a tool called stepper is used.



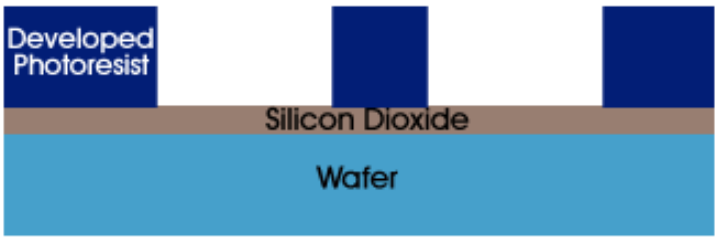
Exposure



Stepper
(ASM Lithography)

IV. Develop and Bake

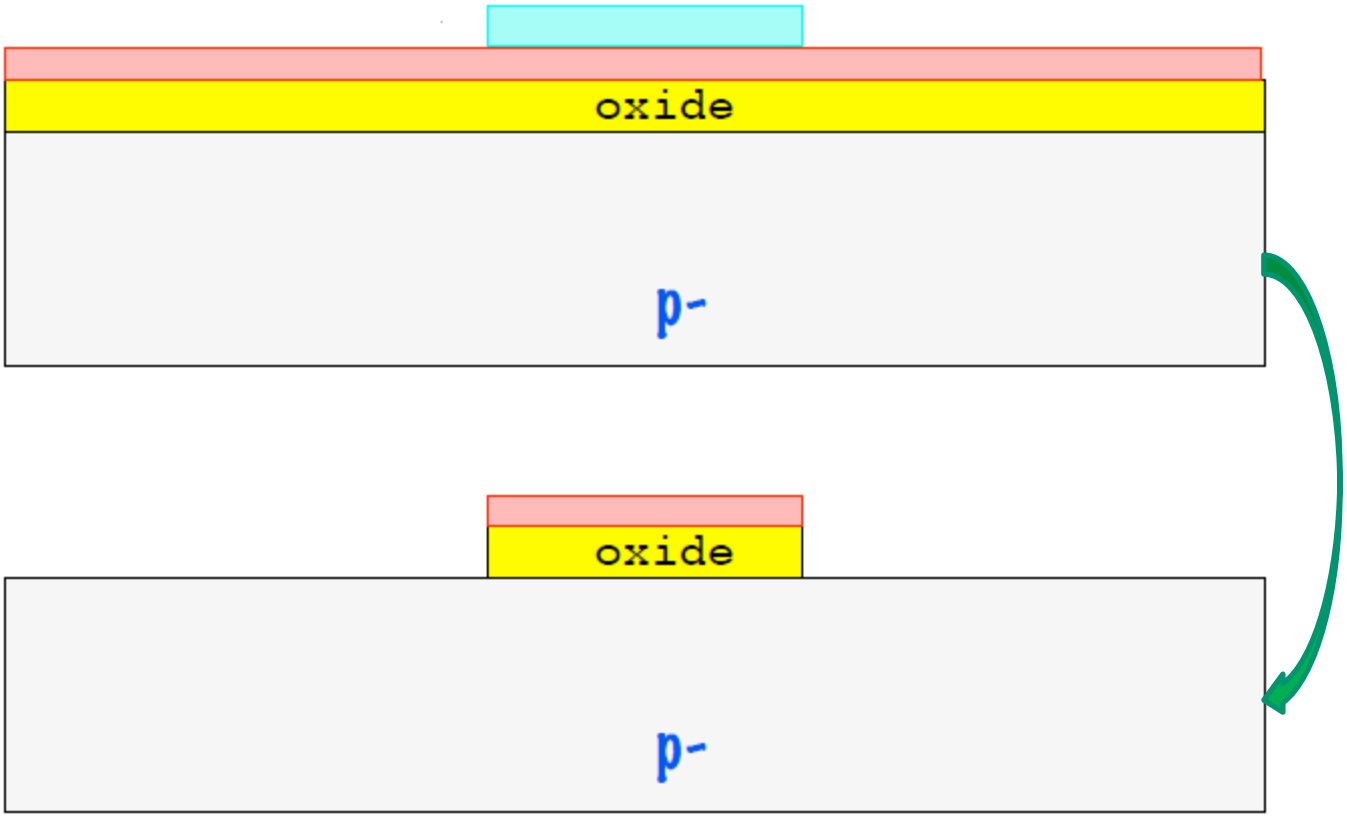
• After exposure, **wafers are developed in either an acid or base solution** to remove the exposed areas of photoresist.
• Once the exposed photoresist is removed, the wafer is "**soft-baked**" at a low temperature to harden the remaining photoresist.



Photoresist Develop & Strip

* Dust particles are the main concern in the photolithography process. Room air quality is measured by Class i.e. a Class 10 room has less than 10 dust particles of size greater than 0.5µm per cubic foot of air. In order to avoid contamination of the wafer surface with dust particles wafer processing is carried out in clean rooms.

2.2.3 Etching



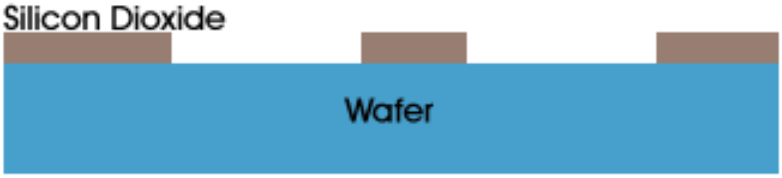
Hydrofluoric (HF) acid etches through poly and oxide, but not hardened resist.

I. Wet and Dry Etch

- Wet etching with chemicals takes place at large wet benches.
- **Different types of acid, base and caustic solutions are used for removing selected areas of different material.**
- **Buffered oxide etch (BOE),** prepared from hydrofluoric acid buffered with ammonium fluoride is used to remove silicon dioxide without etching away underlying silicon or polysilicon layer. BOE is commonly used for more controllable etching.
- Phosphoric acid is used to etch silicon nitride layers.
- Nitric acid is used to etch metals.
- Sulfuric acid is used to remove photoresist.
- **For dry etch, the wafer is placed into an etching chamber and etching is done by plasma.**
- Personnel safety is a primary concern.
- Many fabs use automated equipment perform the etching process.

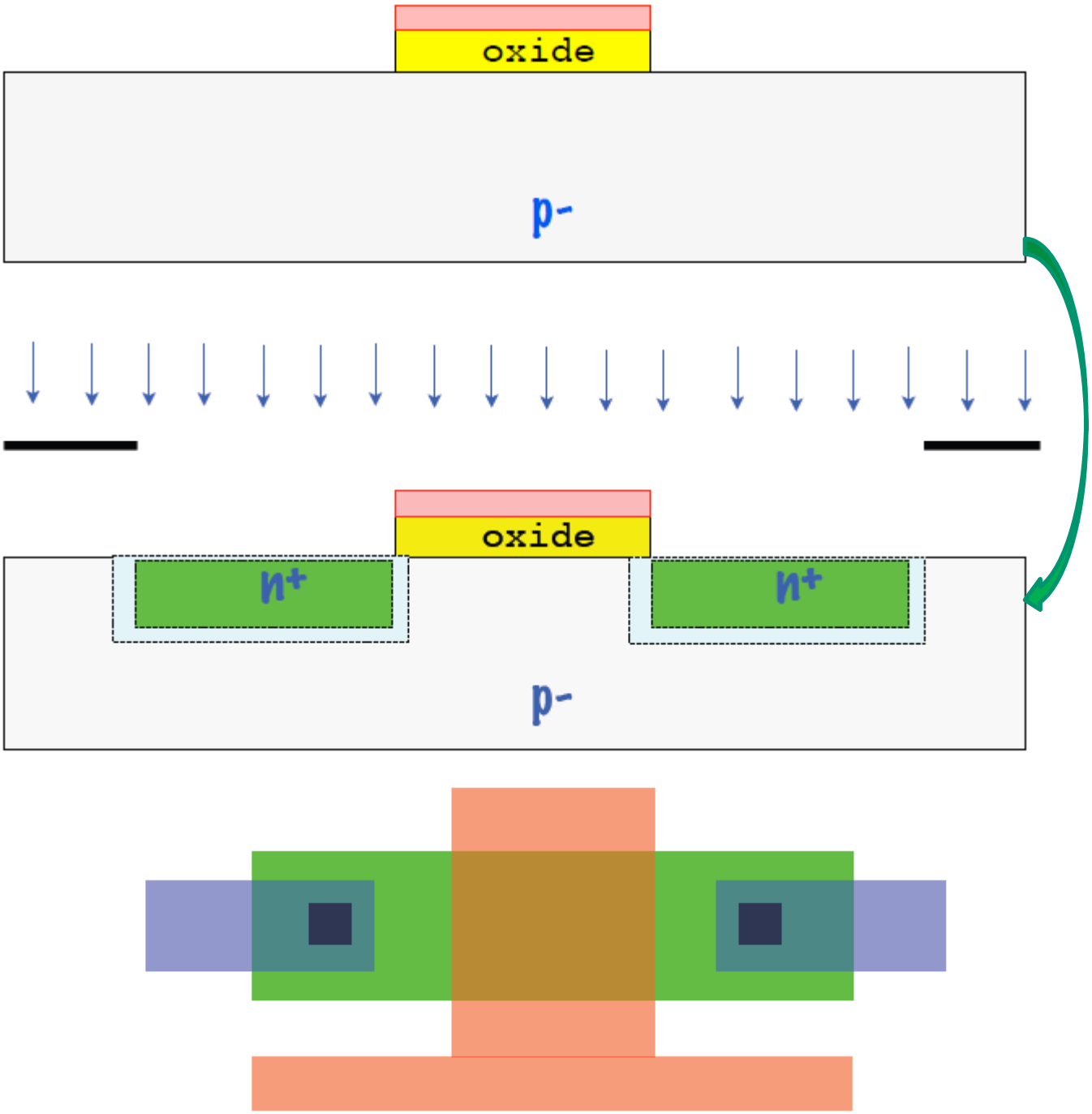
II. Photoresist strip

- The photoresist is then completely stripped off the wafer, leaving the oxide pattern on the wafer.



Oxide Etch

2.2.4 Ion Implantation



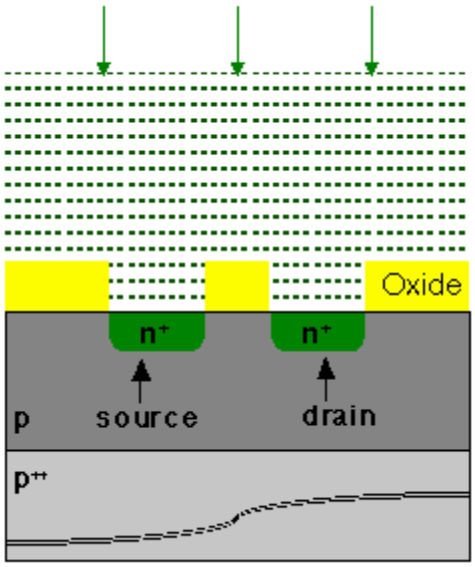
Ion implantation (doping) is the intentional introduction of impurities into an intrinsic semiconductor for the purpose of modulating its electrical, optical and structural properties.

•An ion implanter uses a high-current accelerator tube and steering and focusing magnets to bombard the surface of the wafer with ions of a particular dopant.

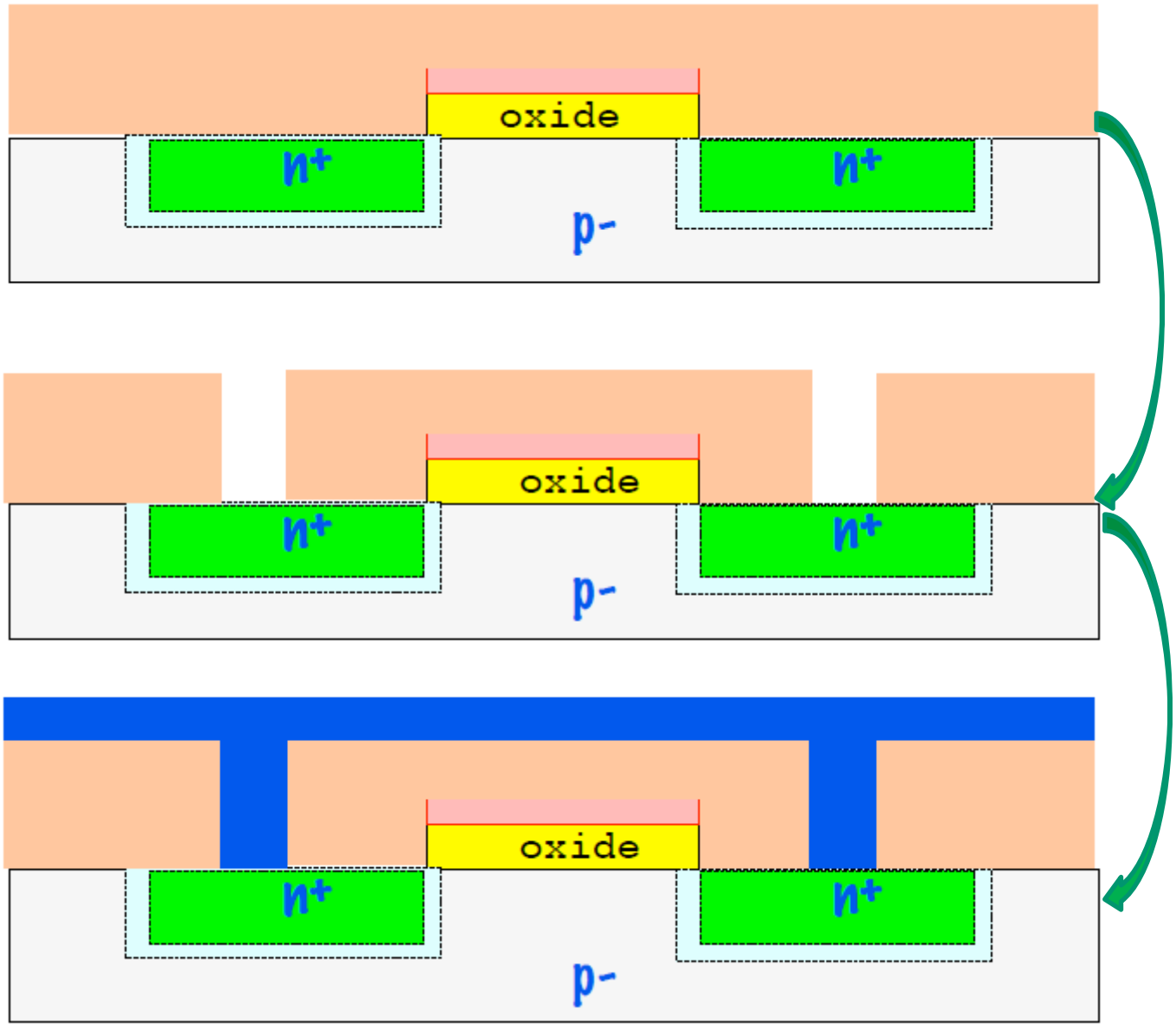
•Common silicon dopants – **Boron (Acceptors, p-type); Phosphorus, Arsenic (Donors, n-type)**

• For the MOSFET example, the oxide acts as a barrier when dopant chemicals are deposited on the surface and diffused into the surface.

• **Annealing** is done by heating the silicon surface to 900°C. The implanted dopant ions diffuse further into the silicon wafer.



2.2.1 Thin Film Deposition (Part B) - Metallization



III. Sputtering

If a target is bombarded with high energy ions such as Ar+ then atoms in the target will be dislodged and transported to the substrate.

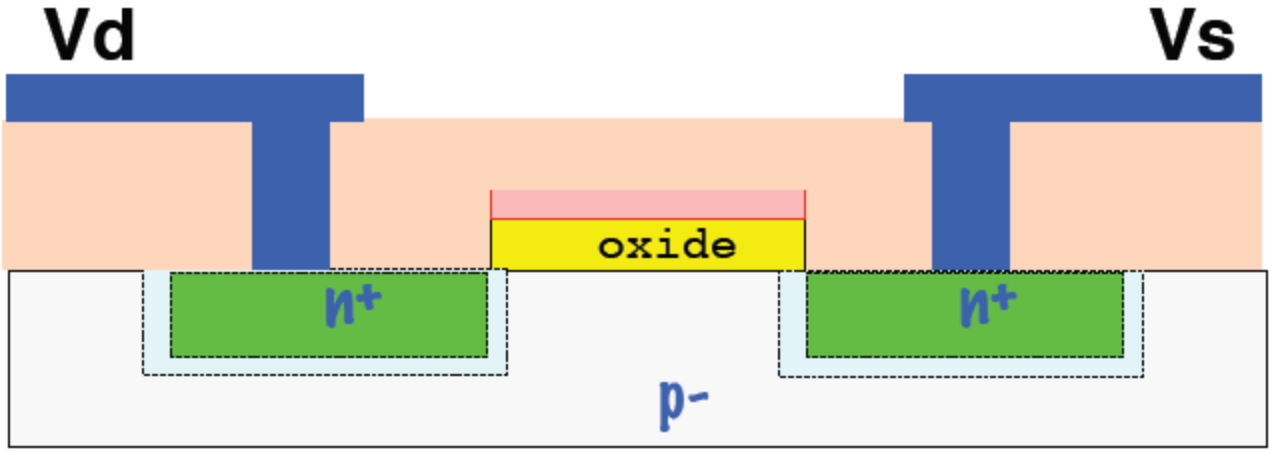
Metals such as Al, Ti can be used as a target.

IV. Evaporation

If Al or Au (gold) is heated to the point of evaporation, then the vapor will condense and form a thin film that covers the surface of the wafer.

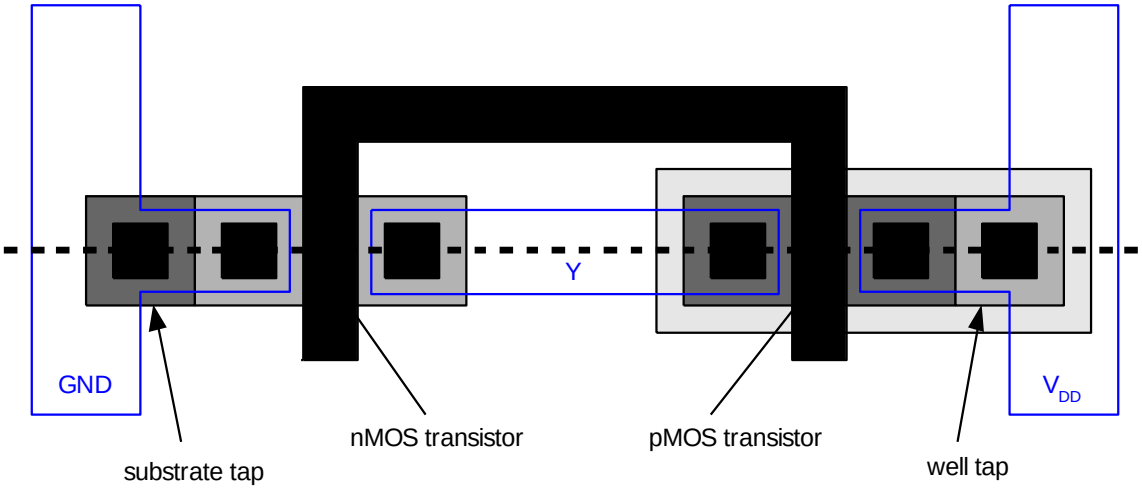
The Semiconductor Manufacturing Process
An n-channel MOS transistor

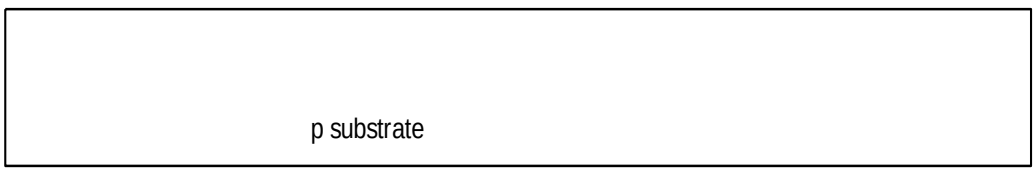
“The planar Process”

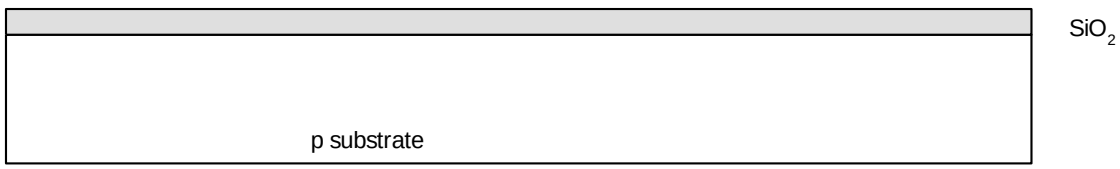


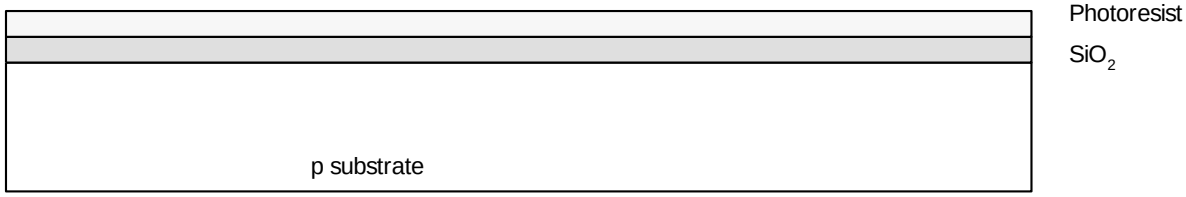
Final product

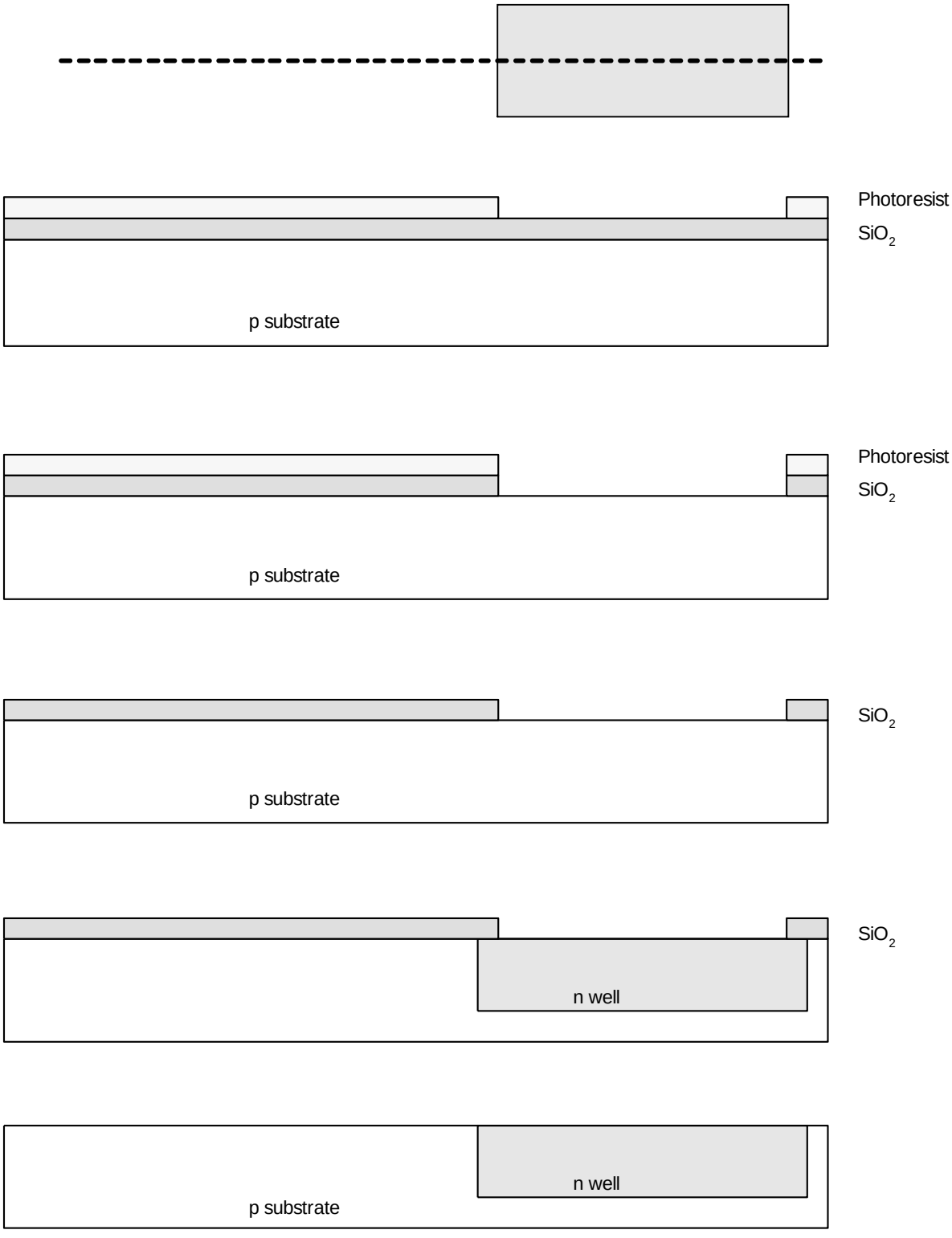
Example: Inverter Mask Set

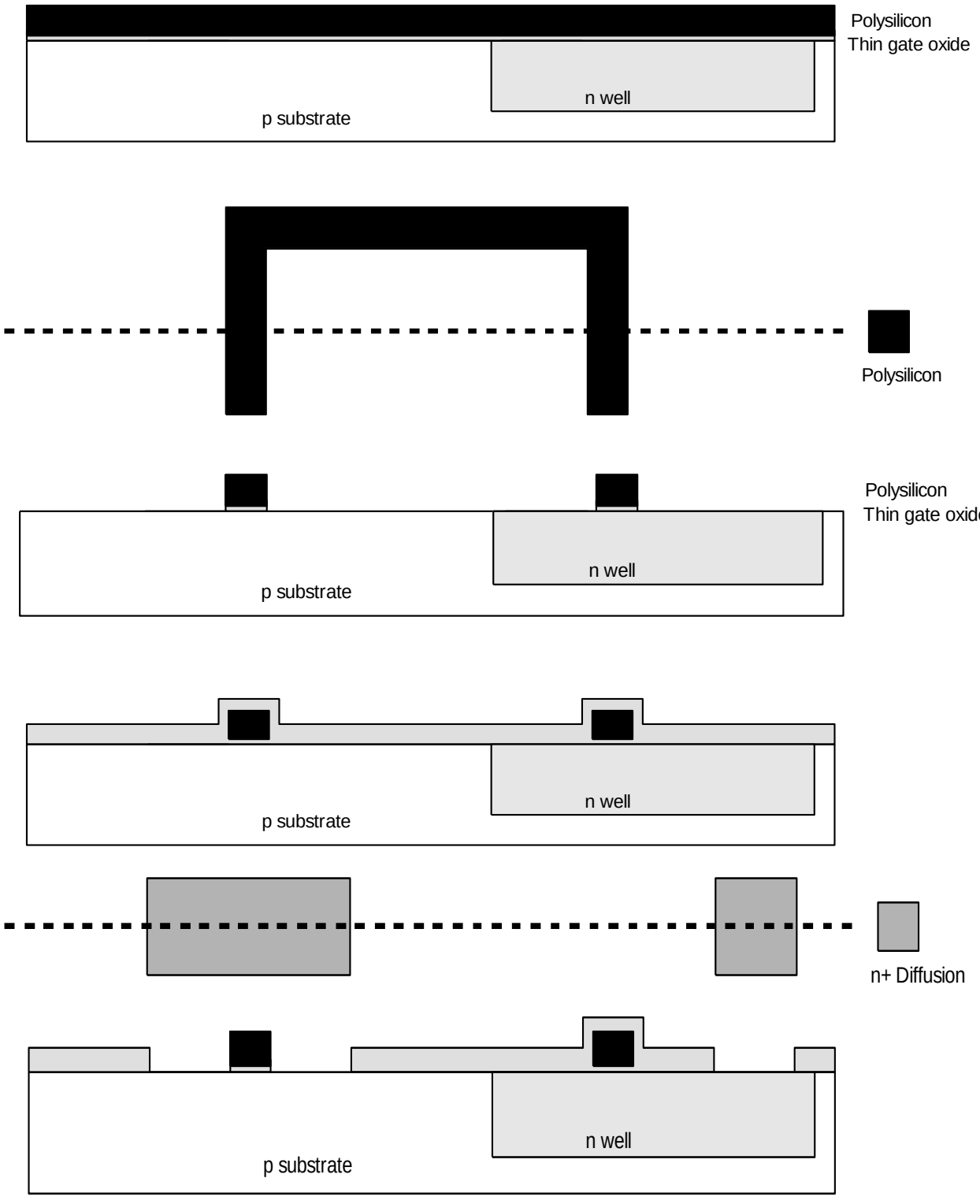


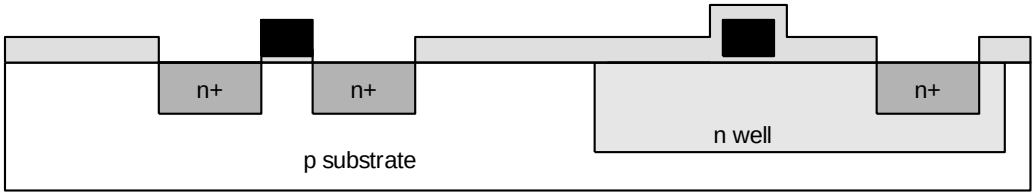


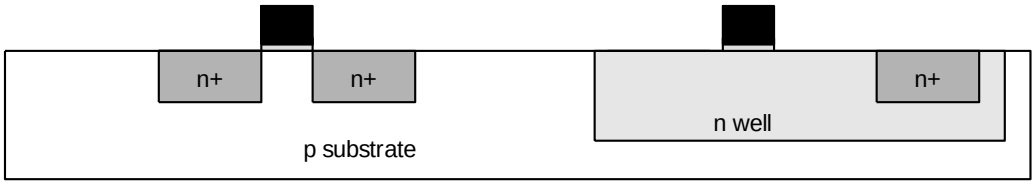


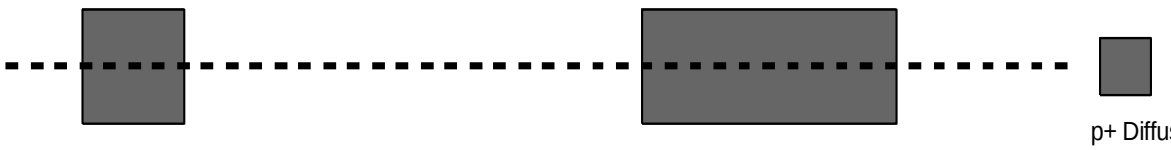


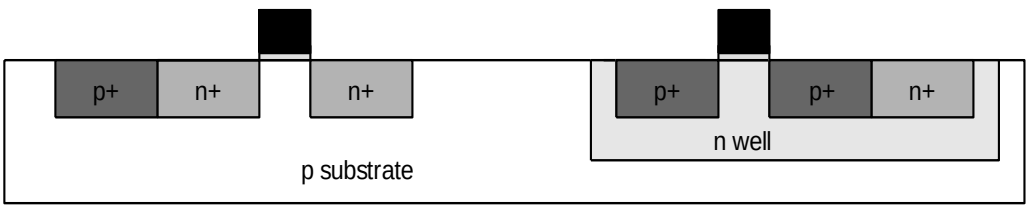

Photoresist
SiO2
p substrate
Photoresist
SiO2
p substrate
SiO2
p substrate
SiO2
n well
n well
p substrate


Polysilicon
Thin gate oxide
n well
p substrate
Polysilicon
Polysilicon
Thin gate oxide
n well
p substrate
n well
p substrate
n+ Diffusion
n well
p substrate

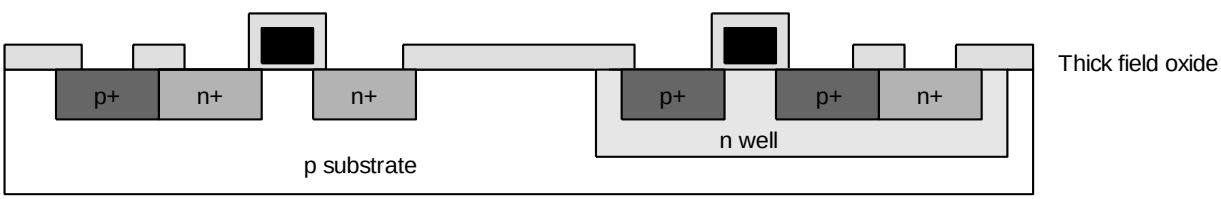

n+
n+
n+
n well
p substrate

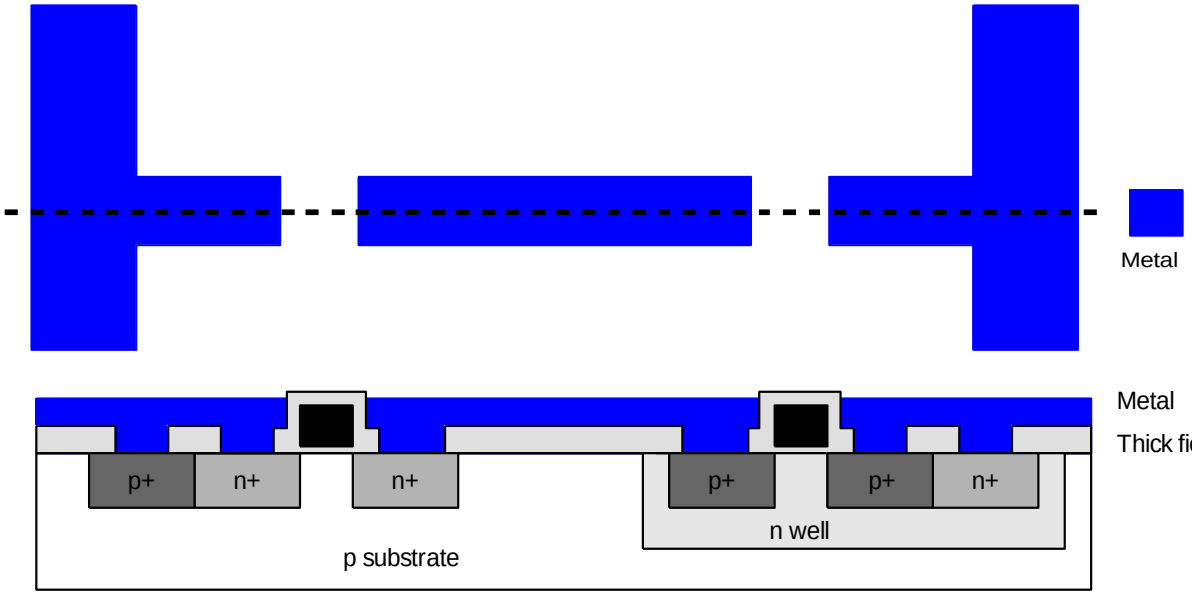

n+
n+
n+
n well
p substrate


p+ Diffusion

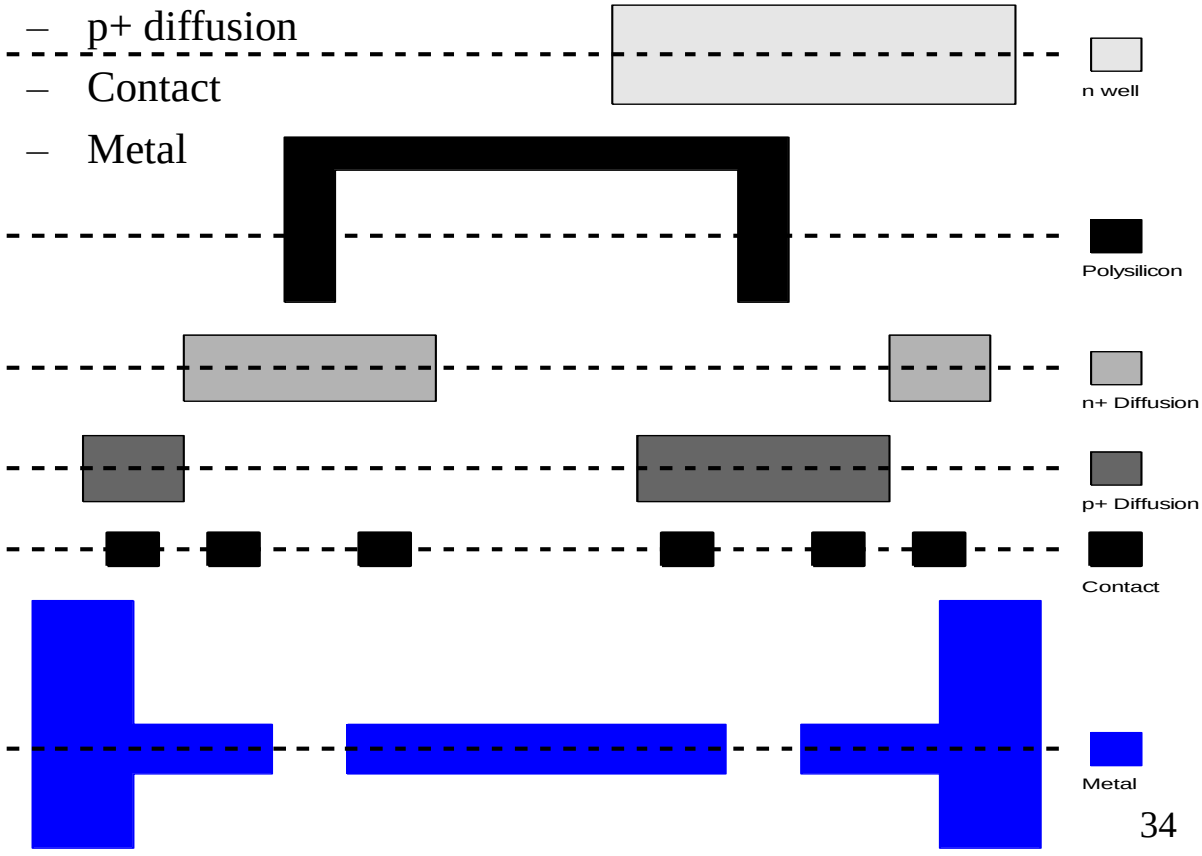

p+
n+
n+
p+
p+
n+
n well
p substrate


Contact


Thick field oxide
p+
n+
n+
p+
p+
n+
n well
p substrate



- Six masks
  - n-well
  - Polysilicon
  - n+ diffusion
  - p+ diffusion
  - Contact
  - Metal



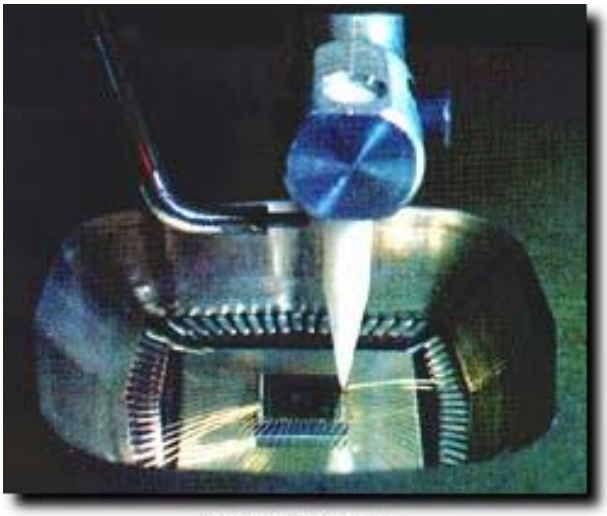
2.3 Post-processing

I. Probe Test and Wafer Dicing

• After the final passivation layer and backside prep, automated methods are used to test the device on the wafer.
• A probe tester is used to check the operation of the device. Devices that fail the test are marked with colored dye.
• After probe test, the wafer is diced into individual die.

II. Wire Bonding and Packing

• Individual devices are attached to a lead frame and aluminum or gold leads are attached via thermal compression or ultrasound welding.
• The packaging is completed by sealing the device into a ceramic or plastic package.

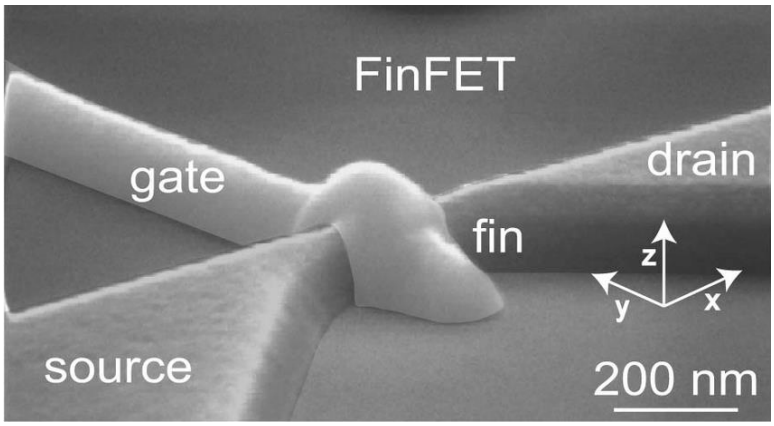


Wire Bonding
(Kulicke & Soffa Industries, Inc.)

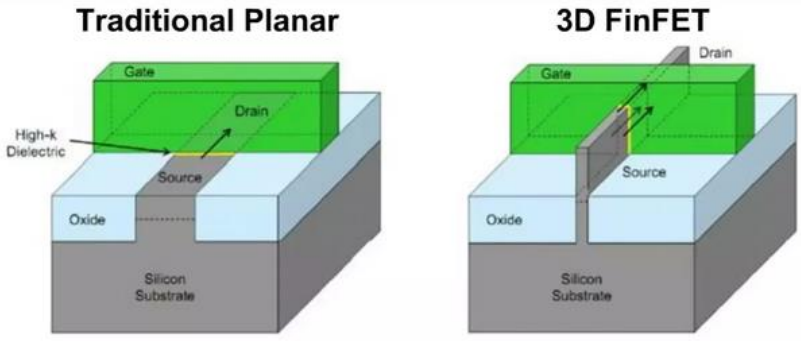
Wire Bonding
(Kaijo Corporation)

Packaging

Additional Reading: Latest fabrication technology



- Transistor channel is a raised fin.
- Gate controls channel from sides and top.



Traditional 2-D planar transistor form a conducting channel in the silicon region under the gate electrode when in the "on" state

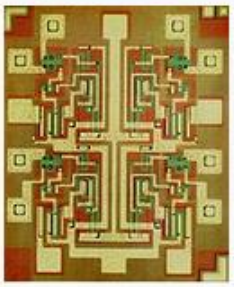
3-D Tri-Gate transistor form conducting channels on three sides of a vertical fin structure, providing "fully depleted" operation

(12) **United States Patent**
Hu et al.

(54) **FINFET TRANSISTOR STRUCTURES HAVING A DOUBLE GATE CHANNEL EXTENDING VERTICALLY FROM A SUBSTRATE AND METHODS OF MANUFACTURE**

(75) Inventors: **Chenming Hu**, Alamo; **Tsu-Jae King**, Fremont; **Vivek Subramanian**, Redwood City; **Leland Chang**, Berkeley; **Xuejue Huang**; **Yang-Kyu Choi**, both of Albany; **Jakub Tadeusz Kedzierski**, Hayward; **Nick Lindert**, Berkeley; **Jeffrey Bokor**, Oakland, all of CA (US); **Wen-Chin Lee**, Beaverton, OR (US)

Semiconductor manufacturing processes



10 µm – 1971
6 µm – 1974
3 µm – 1977
1.5 µm – 1981
1 µm – 1984
800 nm – 1987
600 nm – 1990
350 nm – 1994
250 nm – 1996
180 nm – 1999
130 nm – 2001
90 nm – 2003
65 nm – 2005
45 nm – 2007
32 nm – 2009
22 nm – 2012
14 nm – 2014
10 nm – 2016
7 nm – 2018
5 nm – 2019
3 nm – *~2021*